Control Unit Design

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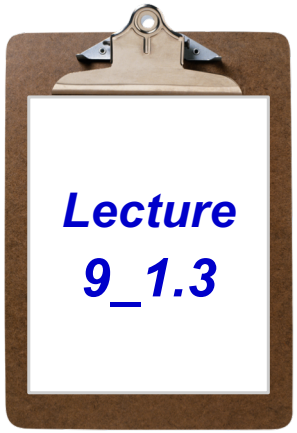

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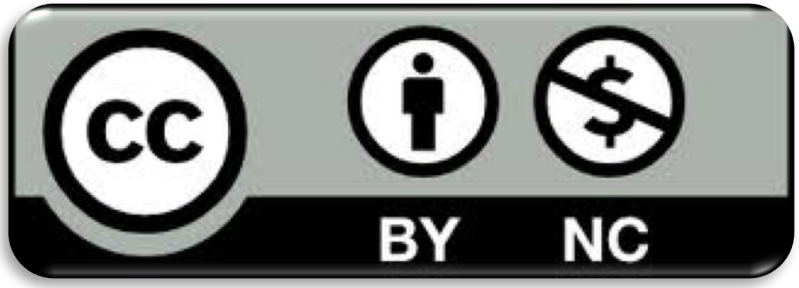

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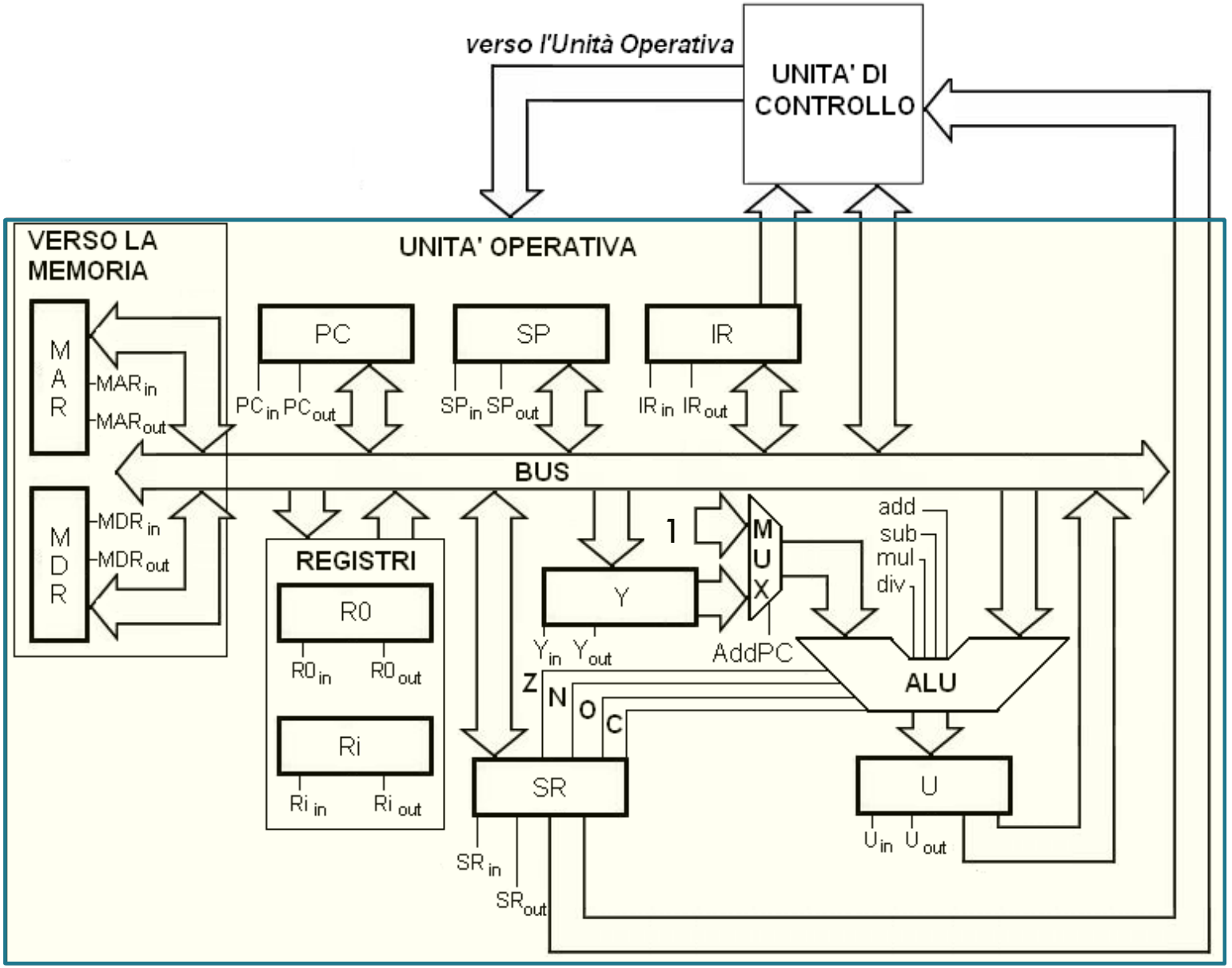
verso l'Unità Operativa
UNITA' DI CONTROLLO
VERSO LA MEMORIA
UNITA' OPERATIVA
MAR
MAR in
MAR out
PC
PC in
PC out
SP
SP in
SP out
IR
IR in
IR out
BUS
MDR
MDR in
MDR out
REGISTRI
R0
R0 in
R0 out
Ri
Ri in
Ri out
1
MUX
Y
Y in
Y out
AddPC
add
sub
mul
div
ALU
Z
N
O
C
SR
SR in
SR out
U
U in
U out

Microfasi

Fetch

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Microfasi

Fetch

1 : MAR <= PC ; U <= PC + 1

2 : Read ; PC <= U

3 : Wait until mem_ready

4 : MDR <= Mem(MAR)

5 : IR <= MDR

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Microfasi

Fetch

1 : MAR <= PC ; U <= PC + 1

2 : Read ; PC <= U

3 : Wait until mem_ready

4 : MDR <= Mem(MAR)

5 : IR <= MDR

LOAD R2,R1

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Microfasi

Fetch

1 : MAR <= PC ; U <= PC + 1

2 : Read ; PC <= U

3 : Wait until mem_ready

4 : MDR <= Mem(MAR)

5 : IR <= MDR

LOAD R2,R1

- 6 : R1 <= R2
- 7 : Jump to 1

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Microfasi

Fetch

1 : MAR <= PC ; U <= PC + 1

2 : Read ; PC <= U

3 : Wait until mem_ready

4 : MDR <= Mem(MAR)

5 : IR <= MDR

LOAD (R2),R1

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Microfasi

Fetch

1 : MAR <= PC ; U <= PC + 1

2 : Read ; PC <= U

3 : Wait until mem_ready

4 : MDR <= Mem(MAR)

5 : IR <= MDR

LOAD (R2),R1

- 6 : MAR <= R2
- 7 : Read
- 8 : Wait until mem_ready
- 9 : MDR <= Mem(MAR)
- 10 : R1 <= MDR
- 11 : Jump to 1

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Microfasi

Fetch

1 : MAR <= PC ; U <= PC + 1

2 : Read ; PC <= U

3 : Wait until mem_ready

4 : MDR <= Mem(MAR)

5 : IR <= MDR

ADD R2,R1

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Microfasi

Fetch

1 : MAR <= PC ; U <= PC + 1

2 : Read ; PC <= U

3 : Wait until mem_ready

4 : MDR <= Mem(MAR)

5 : IR <= MDR

ADD R2,R1

- 6 : Y <= R2
- 7 : U <= Y + R1 ;
  SR <= (Z,N,O,C)
- 8 : R1 <= U
- 9 : Jump to 1

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Microfasi

Fetch

ADD (R2),R1

1 : MAR <= PC ; U <= PC + 1

2 : Read ; PC <= U

3 : Wait until mem_ready

4 : MDR <= Mem(MAR)

5 : IR <= MDR

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Microfasi

Fetch

1 : MAR <= PC ; U <= PC + 1

2 : Read ; PC <= U

3 : Wait until mem_ready

4 : MDR <= Mem(MAR)

5 : IR <= MDR

ADD (R2),R1

- 6 : MAR <= R2
- 7 : Read
- 8 : Wait until mem_ready
- 9 : MDR <= Mem(MAR)
- 10 : Y <= MDR
- 11 : U <= Y + R1 ; SR <= (Z,N,O,C)
- 12 : R1 <= U
- 13 : Jump to 1

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Microfasi (optimized)

Fetch

1 : MAR <= PC ; U <= PC + 1

2 : Read ; PC <= U

3 : Wait until mem_ready

4 : MDR <= Mem(MAR)

5 : IR <= MDR

ADD (R2),R1

- 6 : MAR <= R2
- 7 : Read
- 8 : Wait until mem_ready
- 9 : MDR <= Mem(MAR); Y <= R1
- 10 : U <= Y + MDR ;
- SR <= (Z,N,O,C)
- 11 : R1 <= U
- 12 : Jump to 1

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Microfasi

Fetch

1 : MAR <= PC ; U <= PC + 1

2 : Read ; PC <= U

3 : Wait until mem_ready

4 : MDR <= Mem(MAR)

5 : IR <= MDR

CMP R1,R2

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Microfasi

Fetch

1 : MAR <= PC ; U <= PC + 1

2 : Read ; PC <= U

3 : Wait until mem_ready

4 : MDR <= Mem(MAR)

5 : IR <= MDR

CMP R1,R2

- 6 : Y <= R2
- 7 : U <= Y - R1 ;
  SR <= (Z,N,O,C)
- 8 : Jump to 1

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Microfasi

Fetch

1 : MAR <= PC ; U <= PC + 1

2 : Read ; PC <= U

3 : Wait until mem_ready

4 : MDR <= Mem(MAR)

5 : IR <= MDR

JMP (R2)

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Microfasi

Fetch

1 : MAR <= PC ; U <= PC + 1

2 : Read ; PC <= U

3 : Wait until mem_ready

4 : MDR <= Mem(MAR)

5 : IR <= MDR

JMP (R2)

- 6 : MAR <= R2
- 7 : Read
- 8 : Wait until mem_ready
- 9 : MDR <= Mem(MAR)
- 10 : PC <= MDR
- 11 : Jump to 1

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Microfasi

Fetch

1 : MAR <= PC ; U <= PC + 1

2 : Read ; PC <= U

3 : Wait until mem_ready

4 : MDR <= Mem(MAR)

5 : IR <= MDR

BNE (R2)

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Microfasi

Fetch

1 : MAR <= PC ; U <= PC + 1

2 : Read ; PC <= U

3 : Wait until mem_ready

4 : MDR <= Mem(MAR)

5 : IR <= MDR

BNE (R2)

- 6 : If (SR(Z) = '1') then Jump to 1
- 7 : MAR <= R2
- 8 : Read
- 9 : Wait until mem_ready
- 10 : MDR <= Mem(MAR)
- 11 : PC <= MDR
- 12 : Jump to 1

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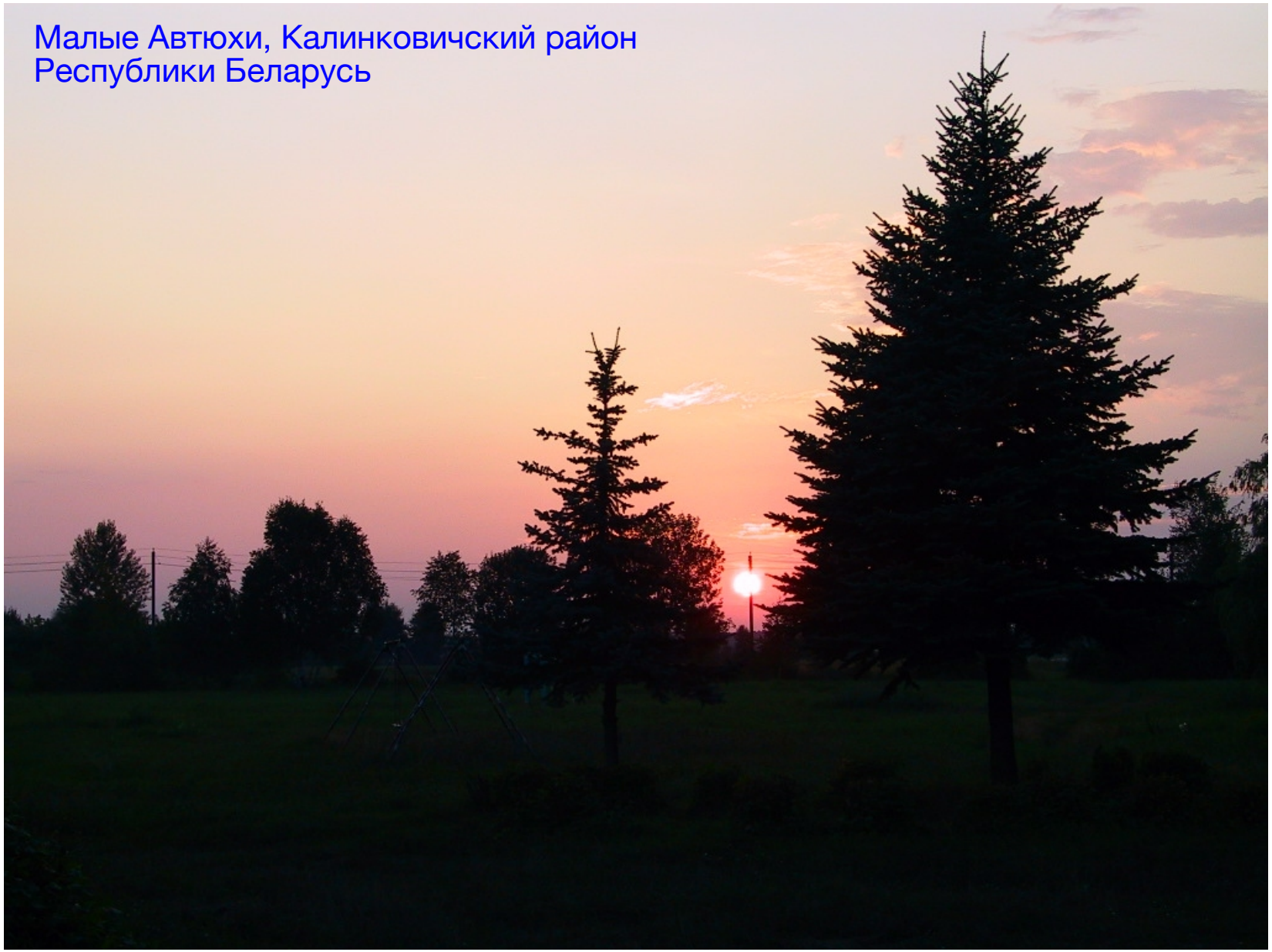

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