Lecture
0_4.4

Digital Network Modeling

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Goal

- The lecture aims at presenting the basic concepts in modeling digital networks, focusing, in particular, on:
  - Combinational vs. sequential
  - Mealy vs. Moore
  - I/O clustering.

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Prerequisites

- Lecture 0_4.2

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Homework

- None

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Further readings

- **Students interested in making a reference to a text book on the arguments covered in this lecture can refer, for instance, to:**
  - ***G. Conte, A. Mazzeo, N. Mazzocca, P. Prinetto*: "Architettura dei calcolatori", *Città Studi, 2015* (Chapter 1: Classificazioni e Concetti base & App. B*: Modellizzazione di circuiti digitali*)) (In Italian)**

Outline

- Combinational vs. sequential networks
- Moore vs. Mealy machines
- I/O clustering

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Outline

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Some graphic conventions

Hereinafter:

——— **will identify a bus or a set of wires**

—— **will identify a single bit wire**

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Model

A model is a simplification of another entity, which can be a physical thing or another model

[Jantsch, 2004]

Model's features

The model contains exactly those characteristics and properties of the modeled entity that are relevant for a given task

Minimal models

A model is minimal with respect to a task if it does not contain any other characteristics than those relevant for the task

Digital network

A proper assembly of electronic devices, designed to store, transform, and communicate information items in digital form

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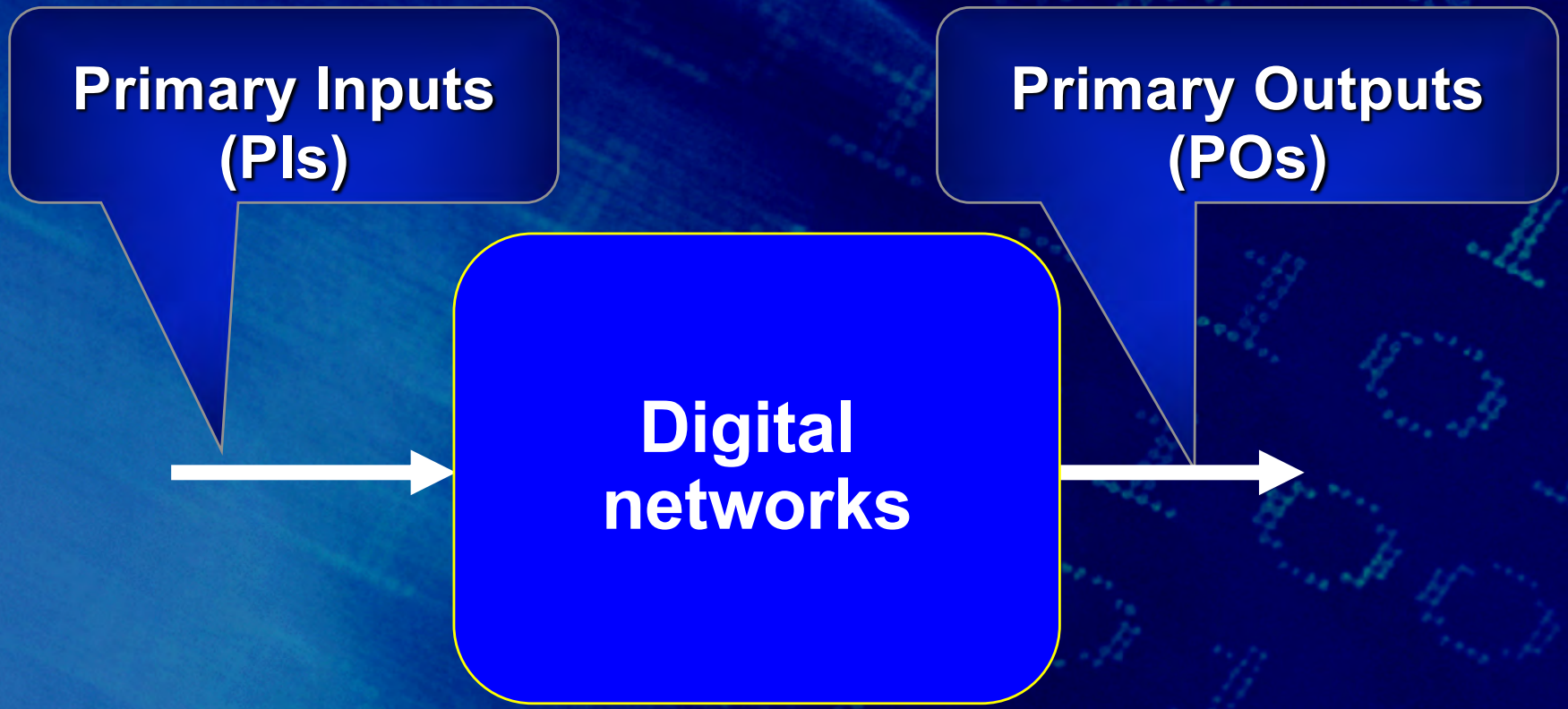

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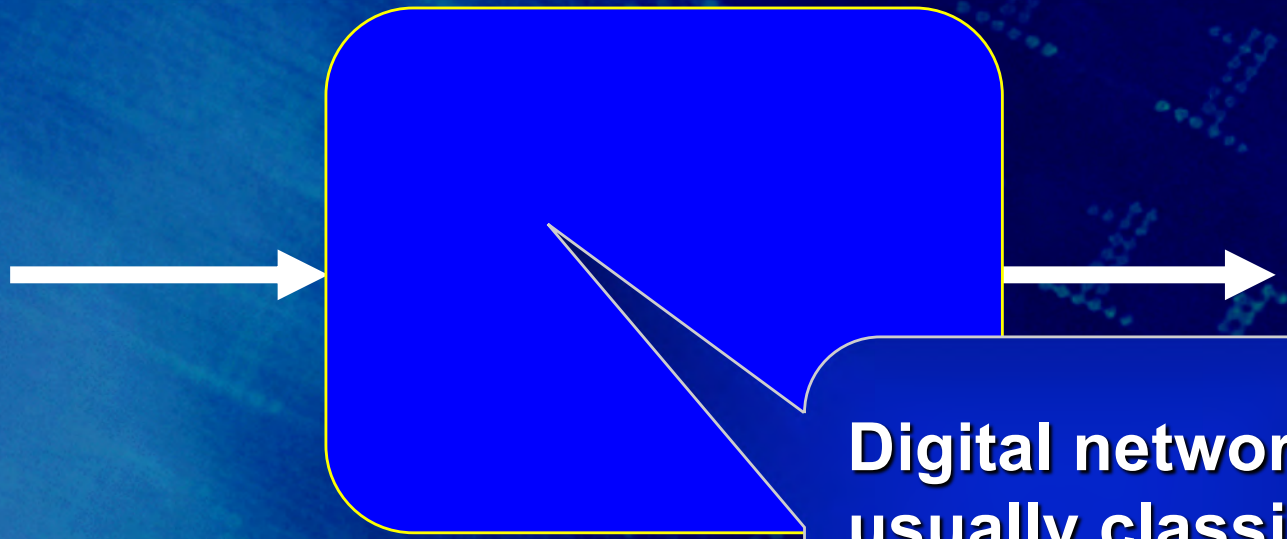
Digital networks classification



Digital networks are usually classified as:

- **combinational**
- **sequential**

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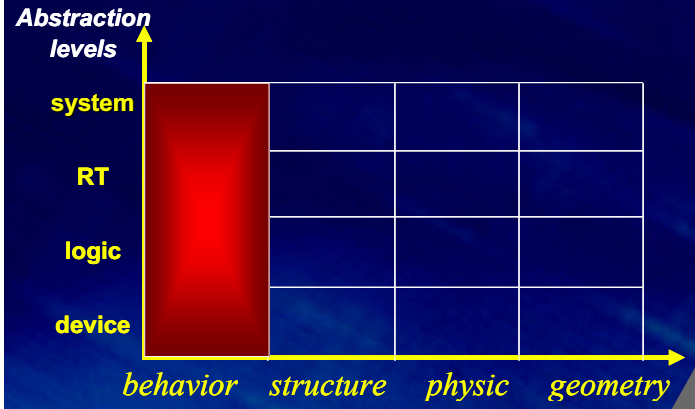

Combinational network

A digital network is **combinational** iff its POs are completely determined by its present PIs, only

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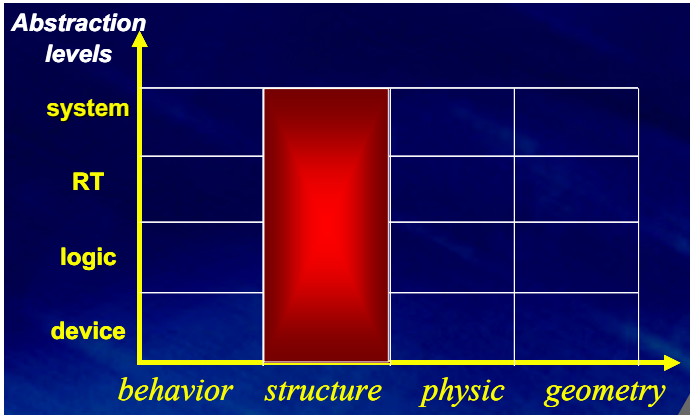

Combinational network

A digital network is **combinational** iff its netlist doesn't contain any feedback loop

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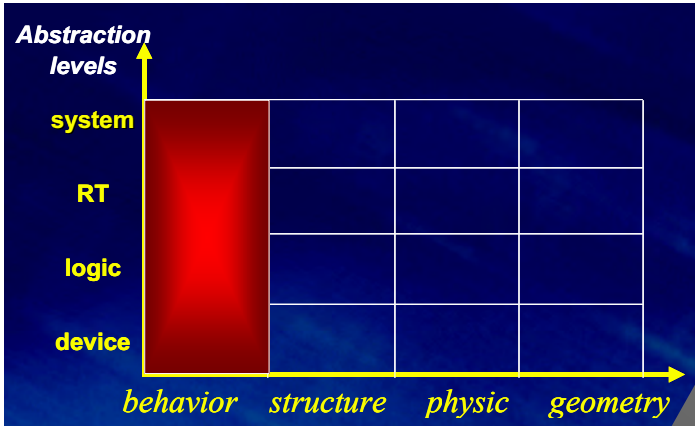

Sequential network

A digital network is **sequential** if its POs are a function of past as well as present values of the PIs

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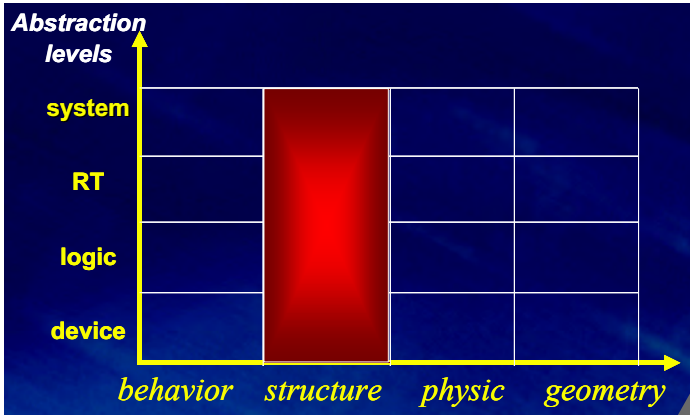

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Sequential network

A digital network is **sequential** if its netlist contains one, or more, feedback loops

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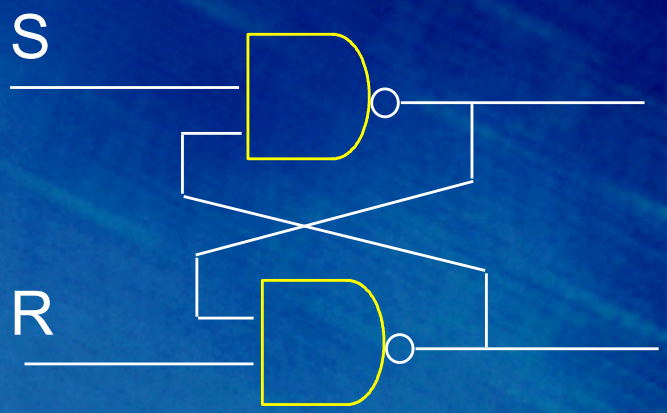
An example



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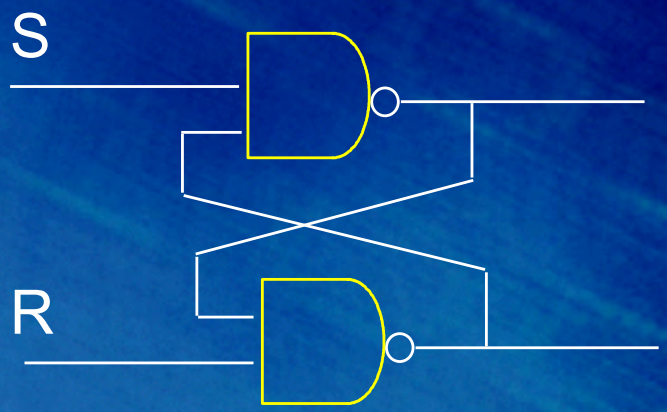
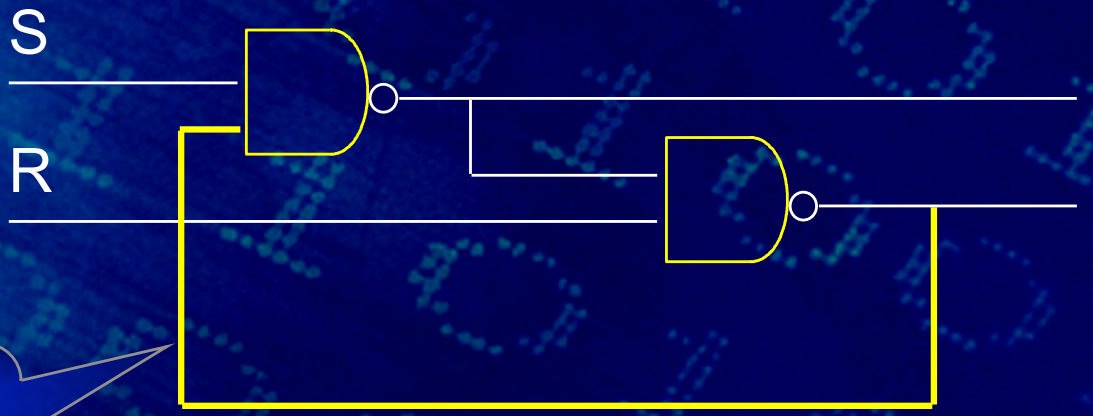
An example





Feedback

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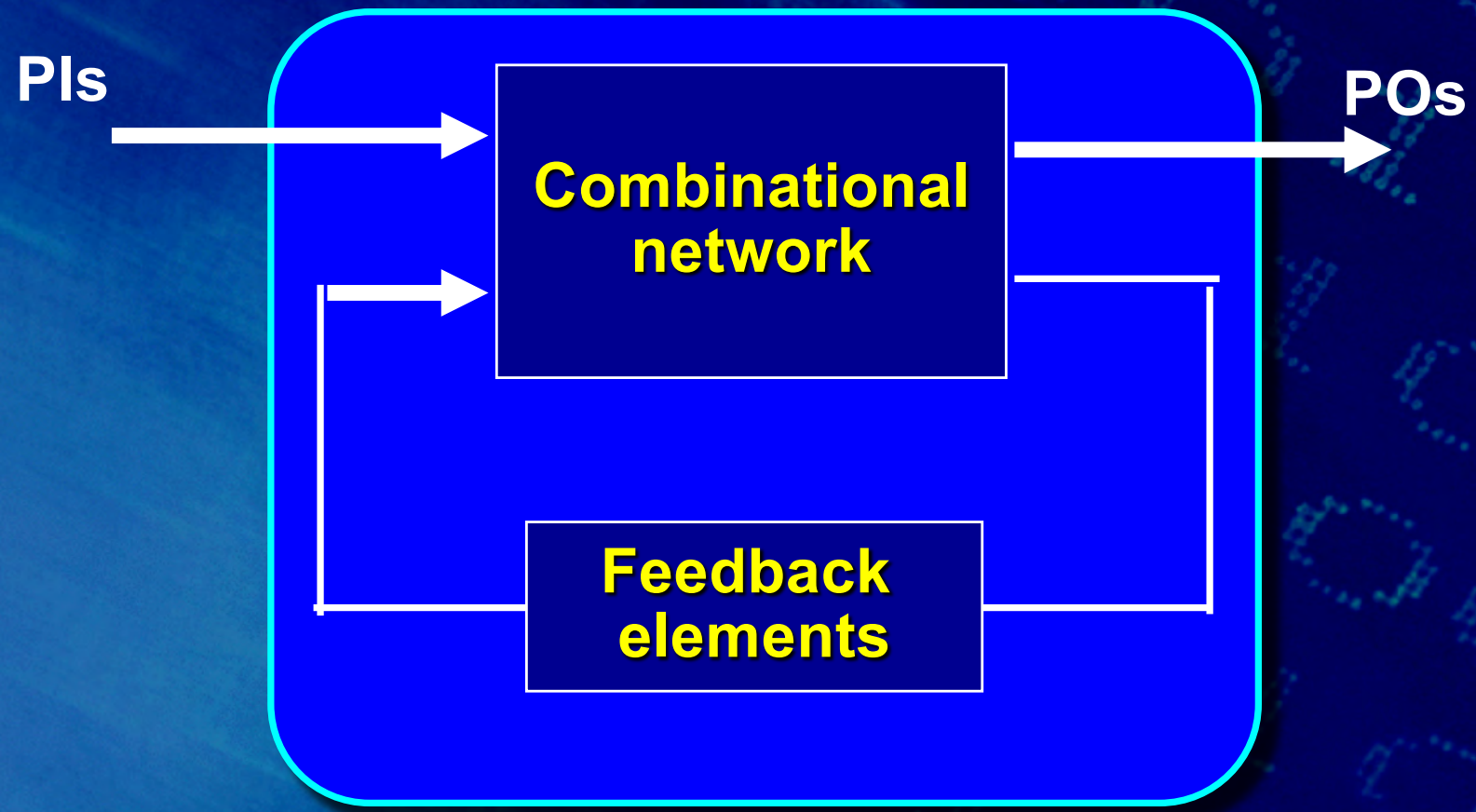
General structure of a sequential network



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The concept of state

- **A sequential circuit must be able to “remember”, or “store”, some information items related to the values the PIs have got.**
- **Such a storing capability is accomplished in terms of “*internal states*”: in any instant, the circuits is in a well defined “state”, univocally represented by the values got by the set of “internal state variables”.**

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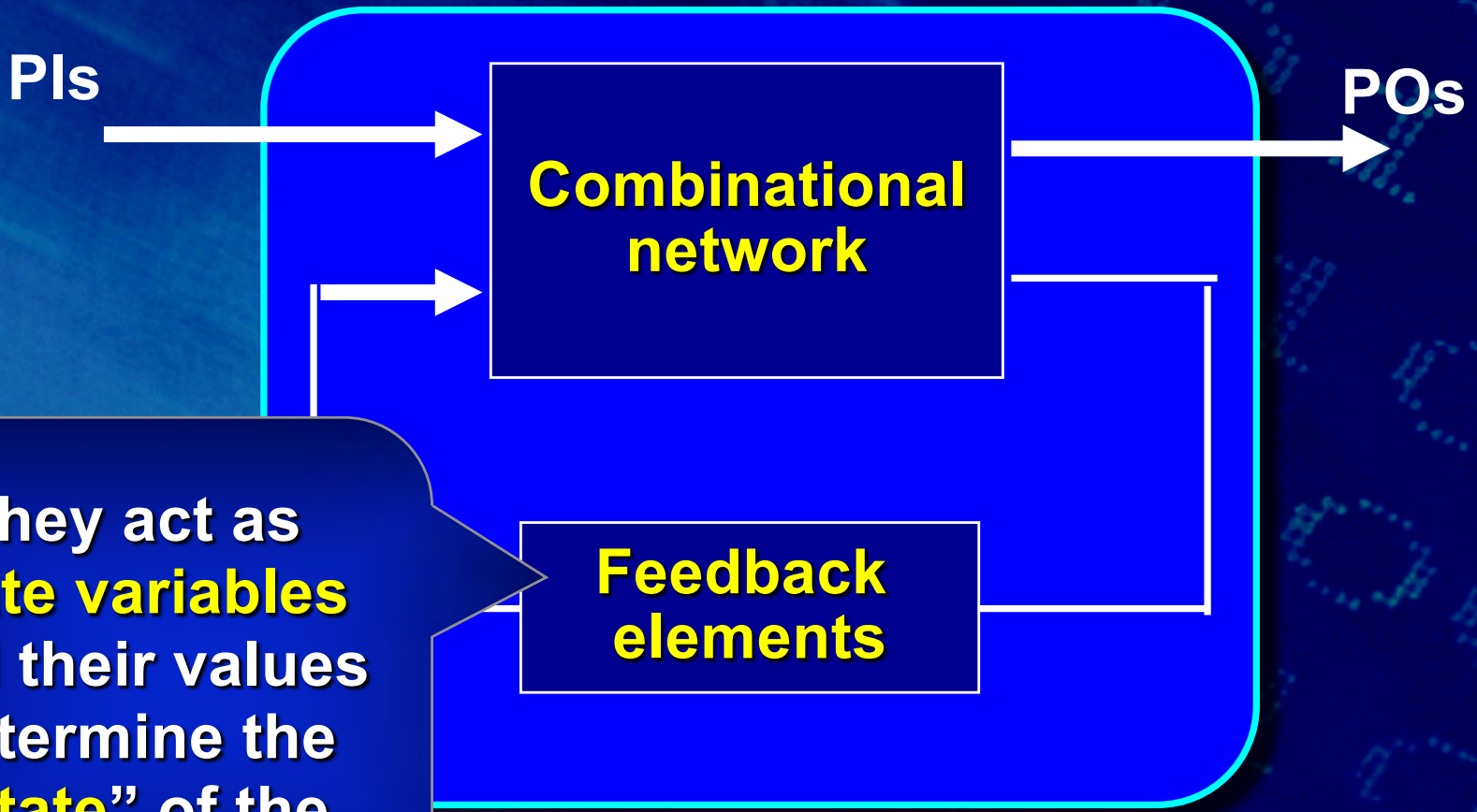
General structure of a sequential network



They act as **state variables** and their values determine the "**state**" of the network

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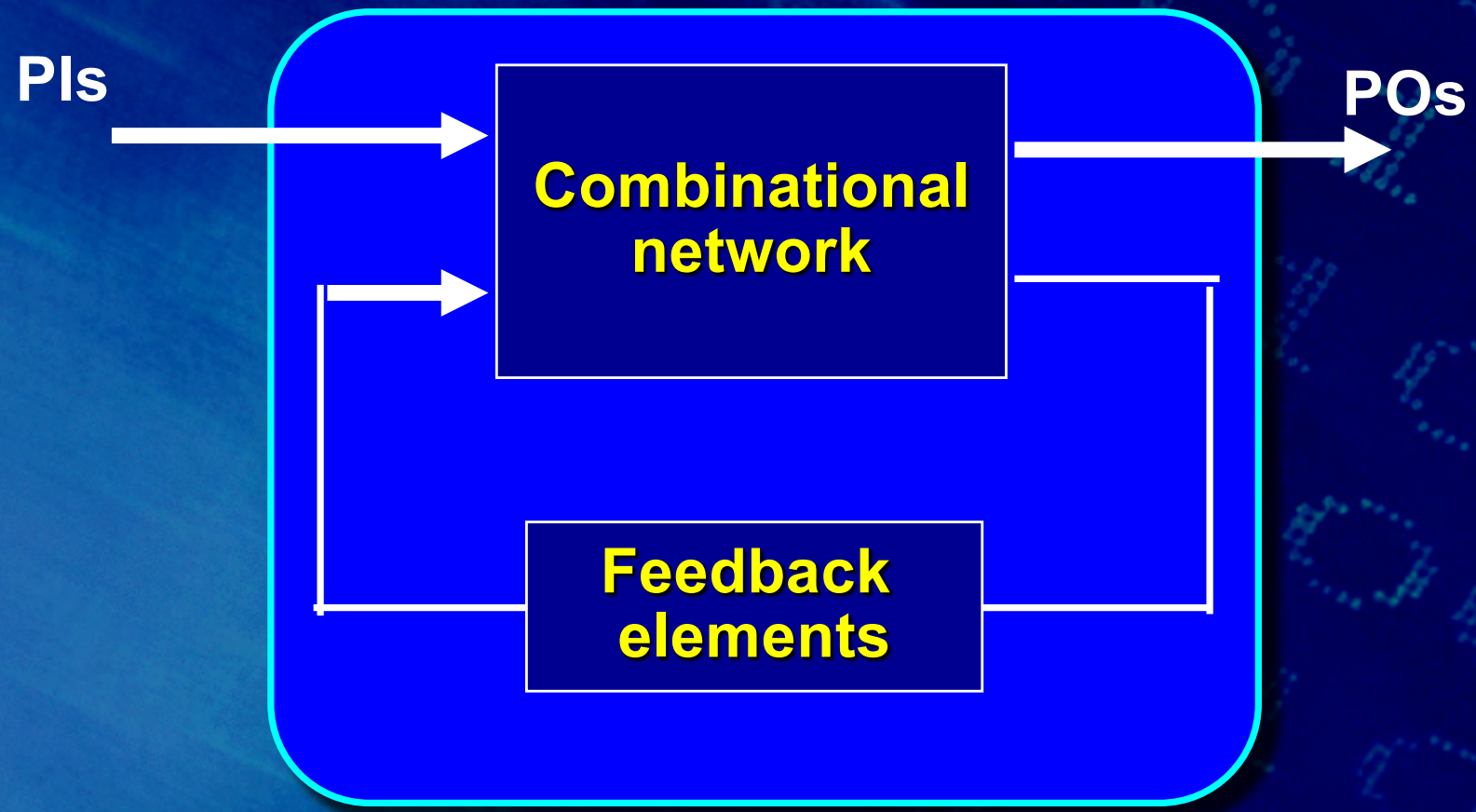
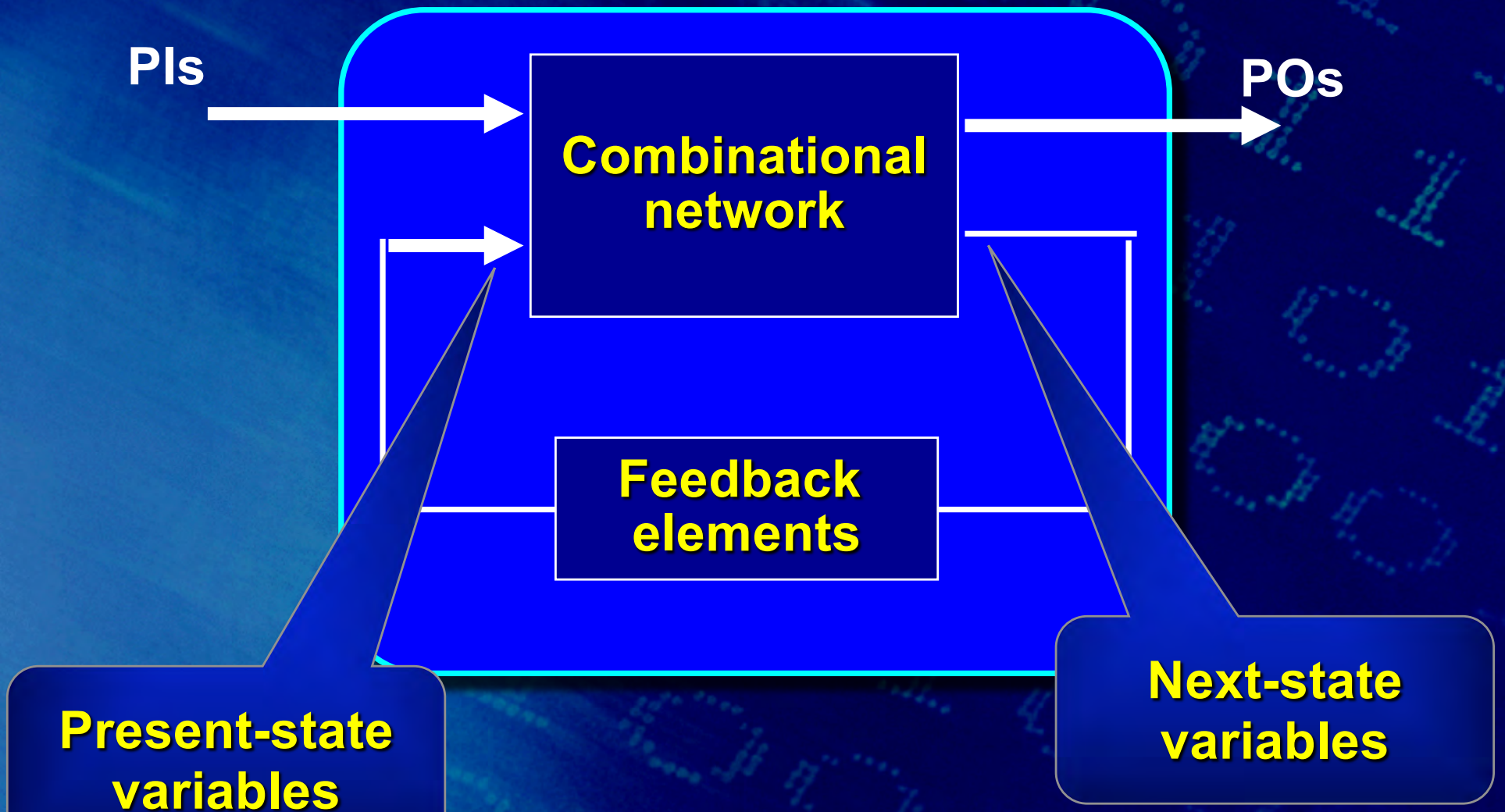
General structure of a sequential network



General structure of a sequential network



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State variables

- A sequential network has as many state variables as feedback elements
- Each state variables can get *2* possible values
- A network with *n* state variables is characterized by 2^n possible states.

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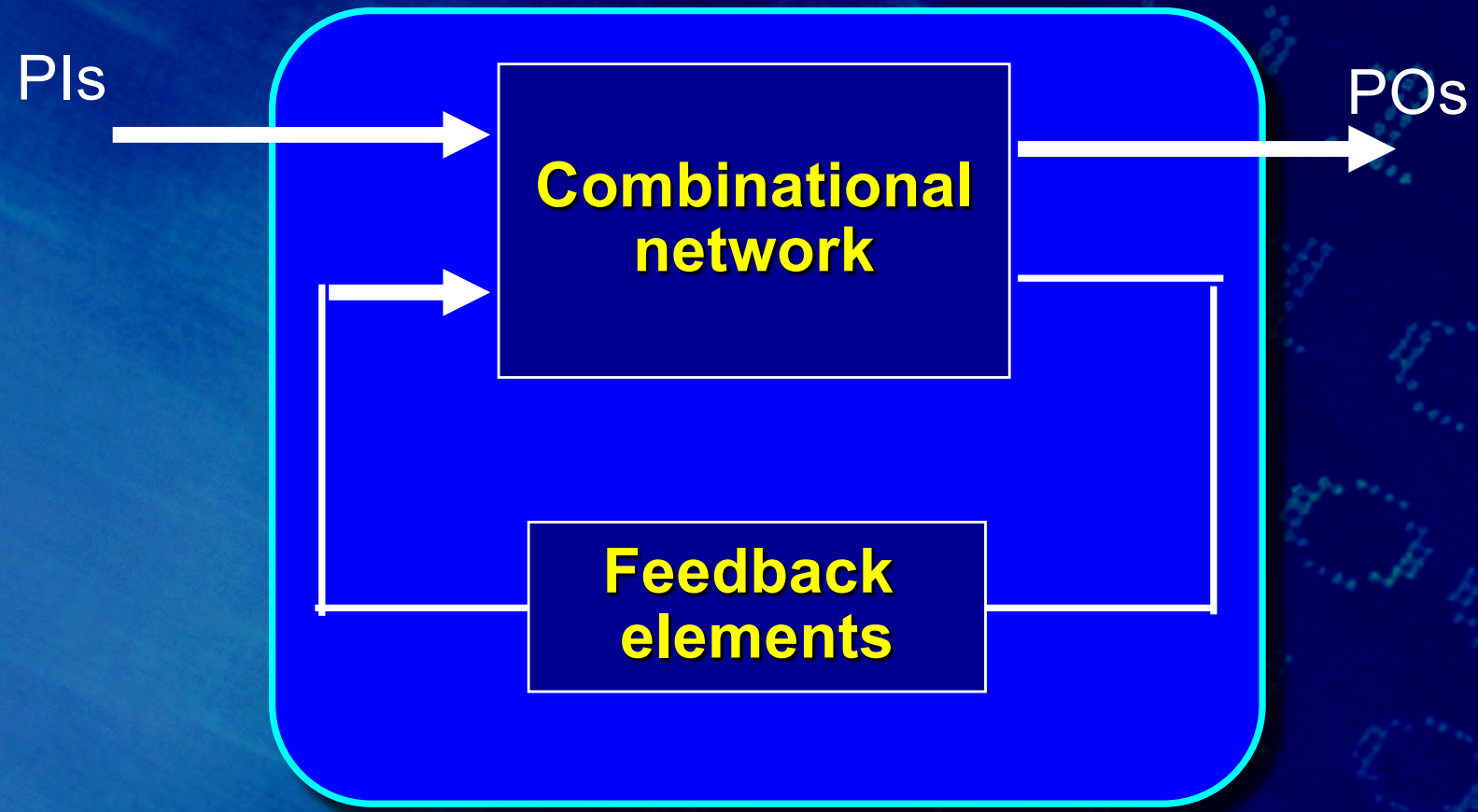
Sequential network classification



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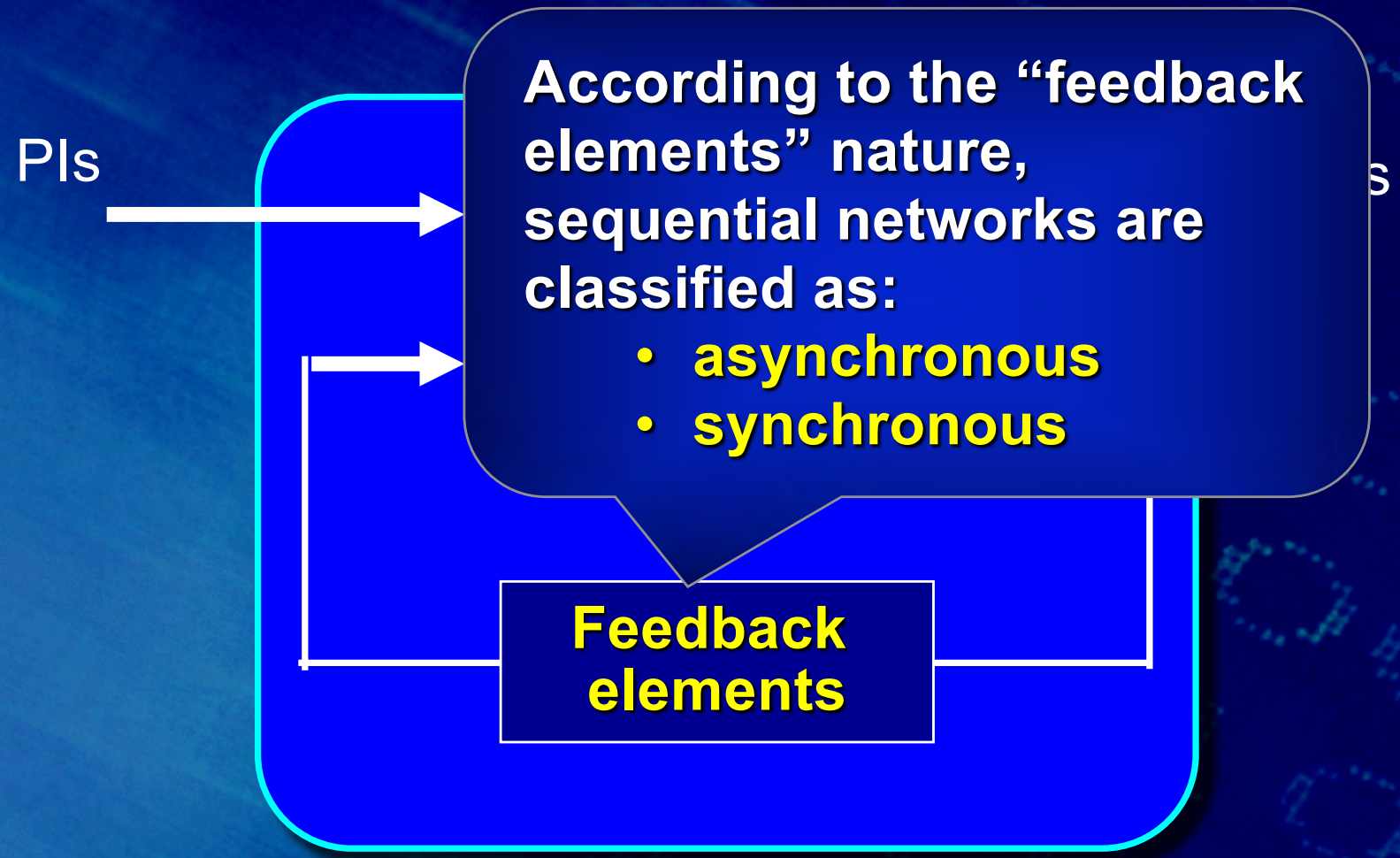
Sequential network classification



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Asynchronous networks

- Each feedback element is just a wire
- The information flows through feedback elements is a continuum and not ***synchronized*** by any external event

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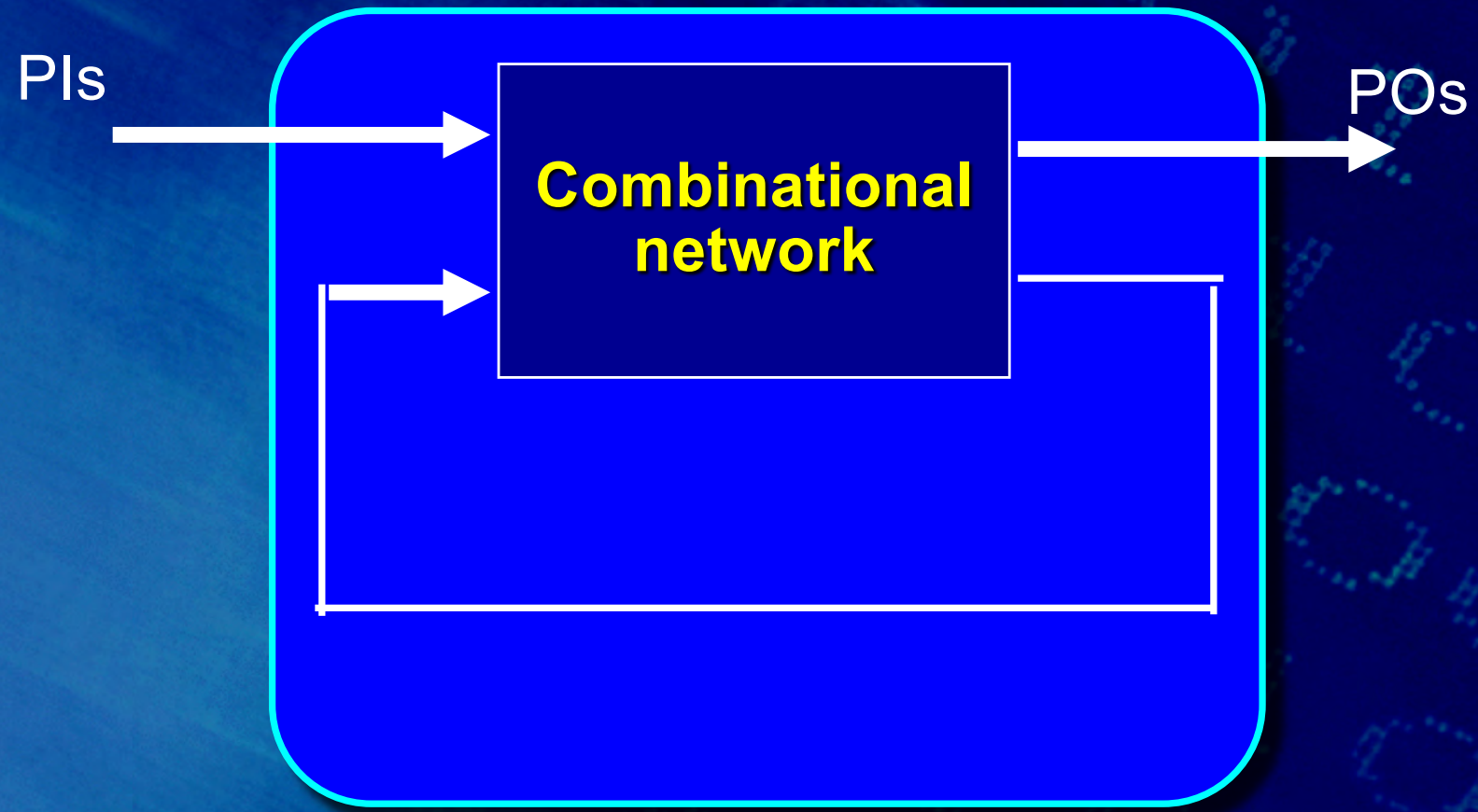
Asynchronous network structure



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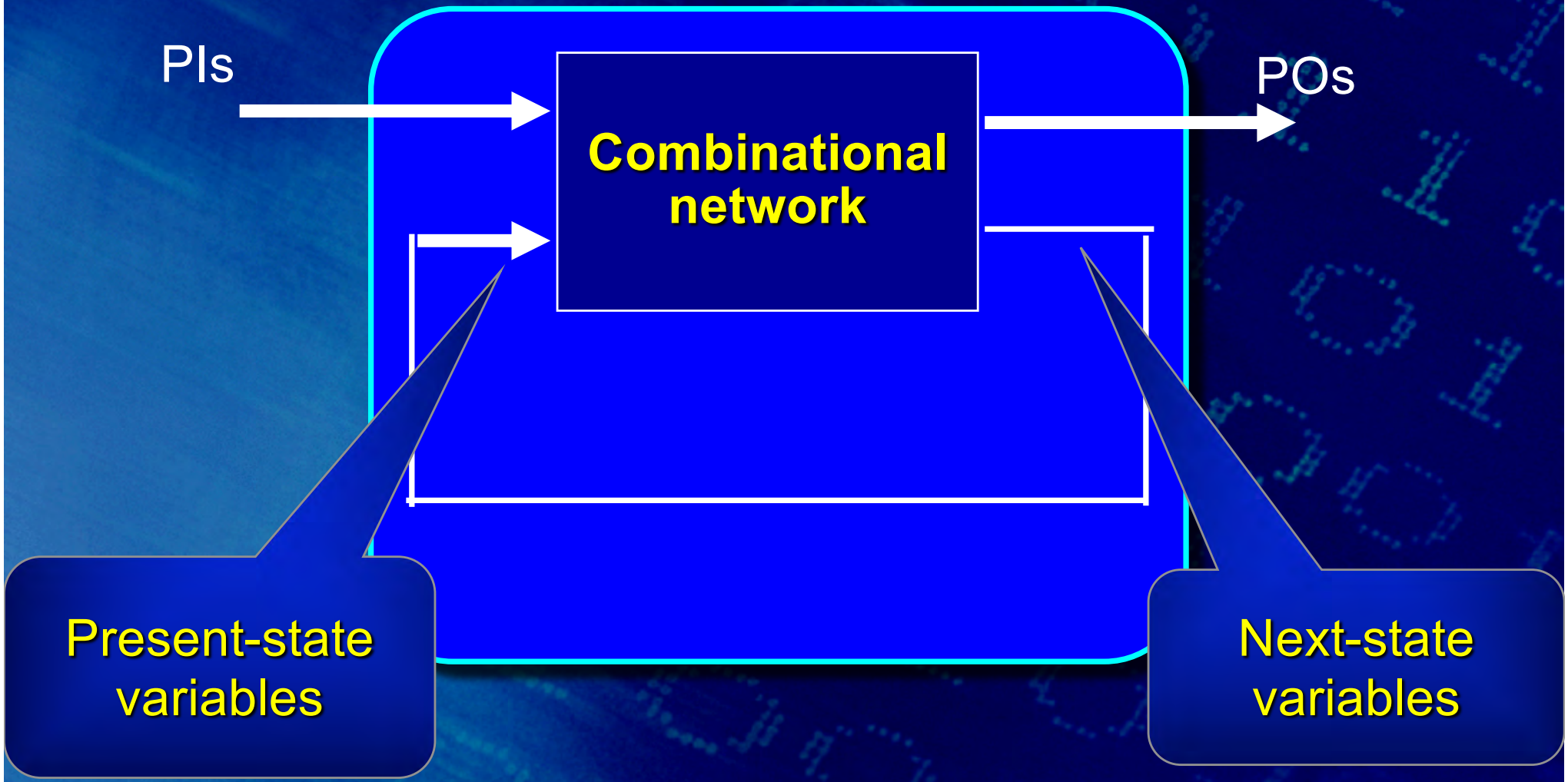
Asynchronous network structure



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Synchronous networks

- Each feedback is always performed via a particular device, named ***Flip-Flop***
- Flip-Flop behavior is controlled and timed by an ad-hoc signal, usually referred to as ***clock***
- The information flow through the feedback elements is thus “synchronized” by the ***clock***

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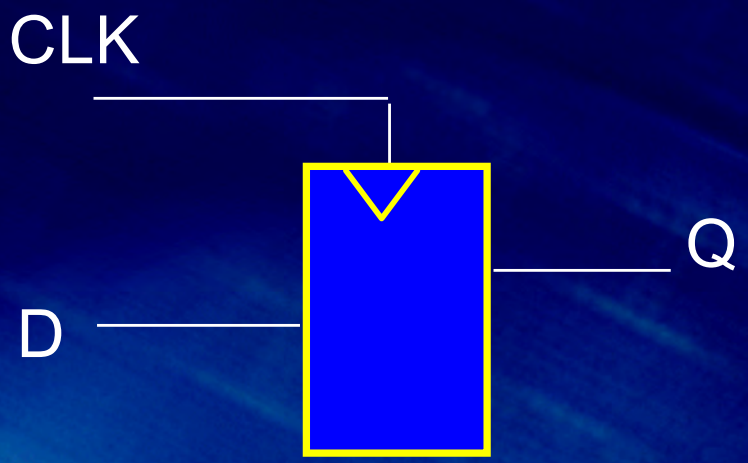
Flip-Flop behavior



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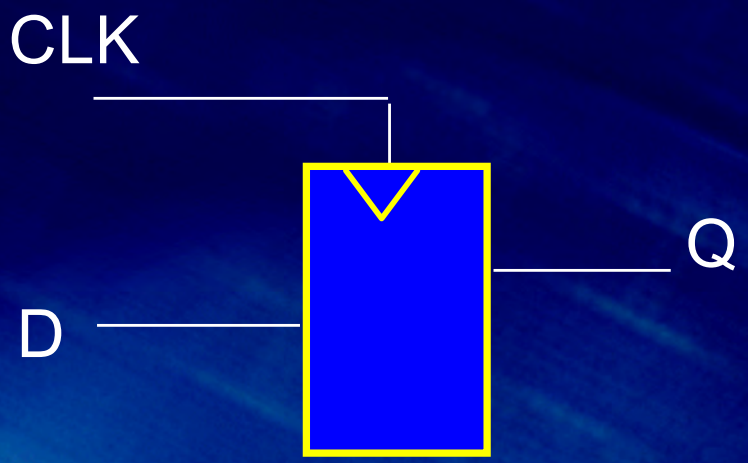
Flip-Flop behavior



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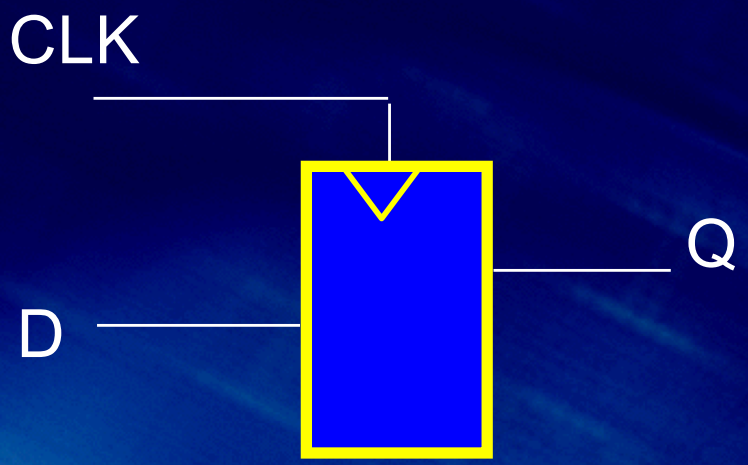
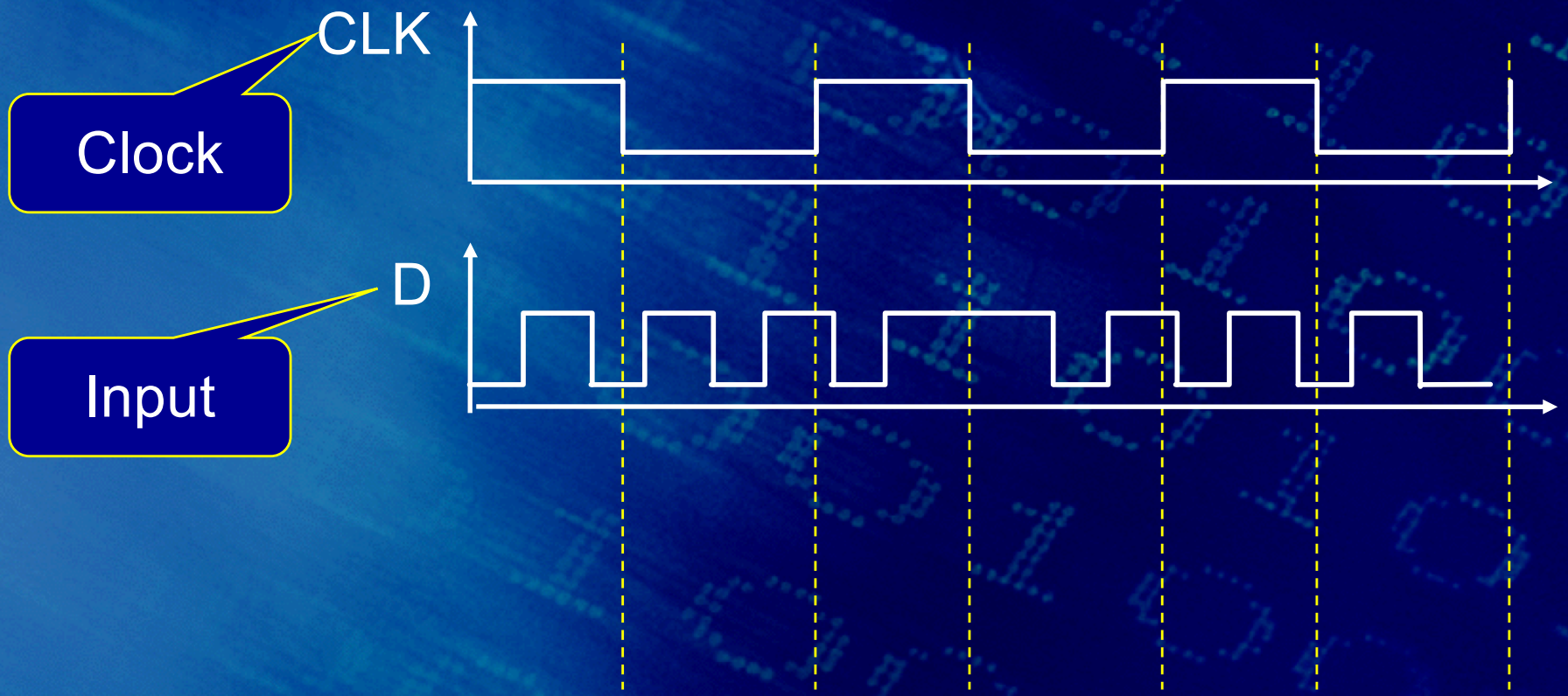
Flip-Flop behavior





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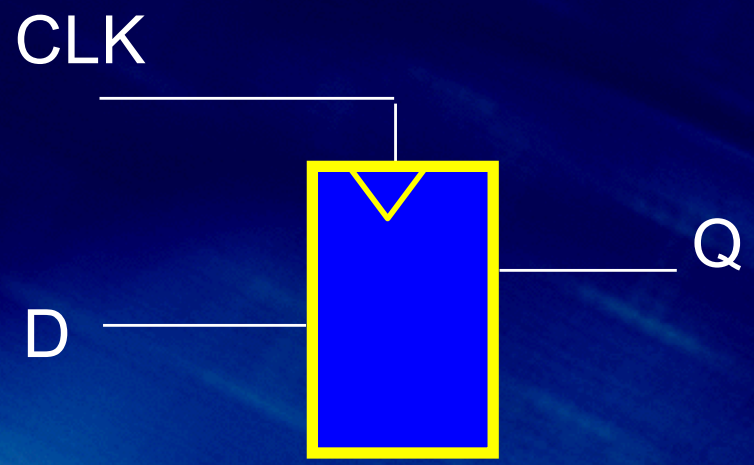
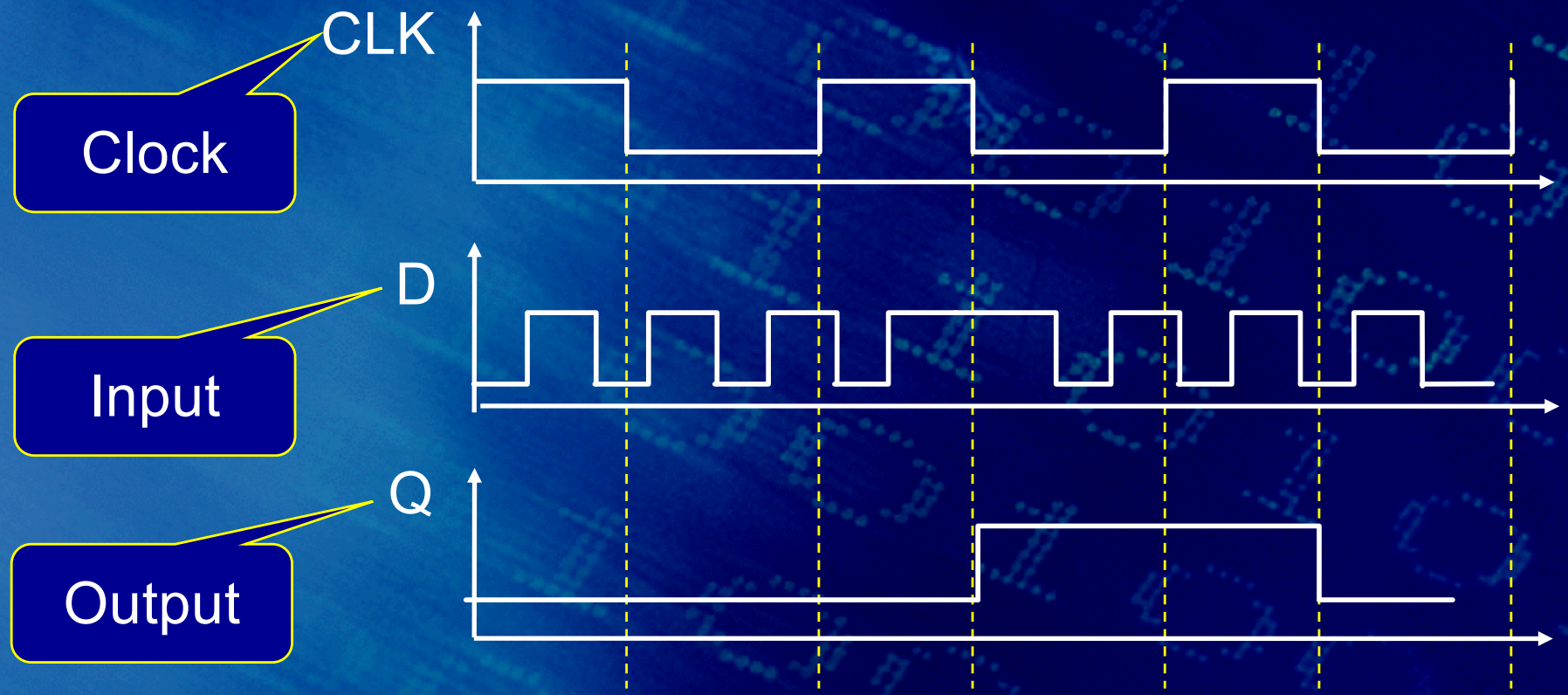
Flip-Flop behavior





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State register

- **The set of Flip-Flops is often referred to as "*State Register*", since it stores the network state variables.**

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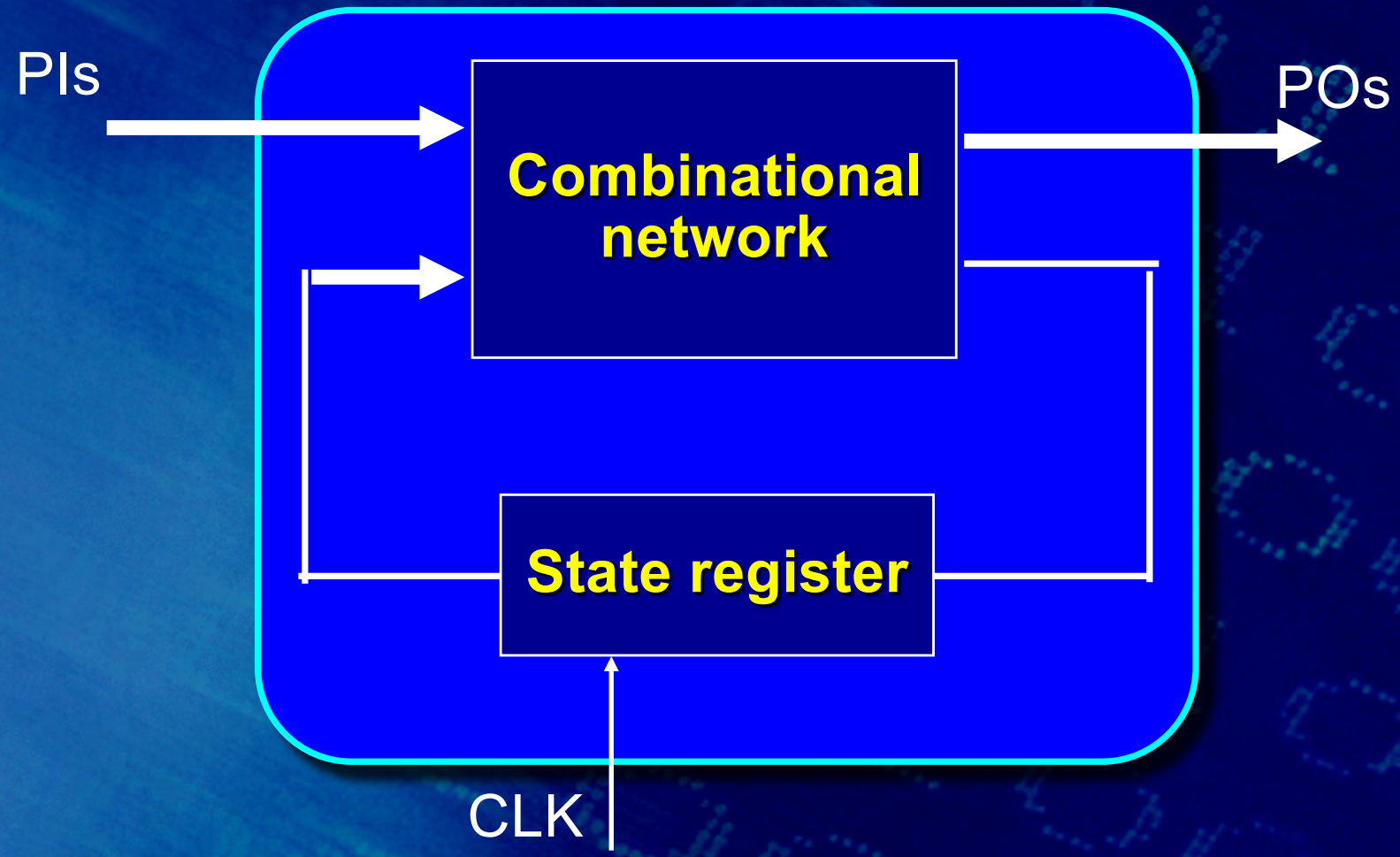
Synchronous network structure



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Finite State Machines

- **Synchronous networks, being characterized by a finite # of flip-flops, and thus of states, are very often referred to as *Finite State Machines* (FSMs).**

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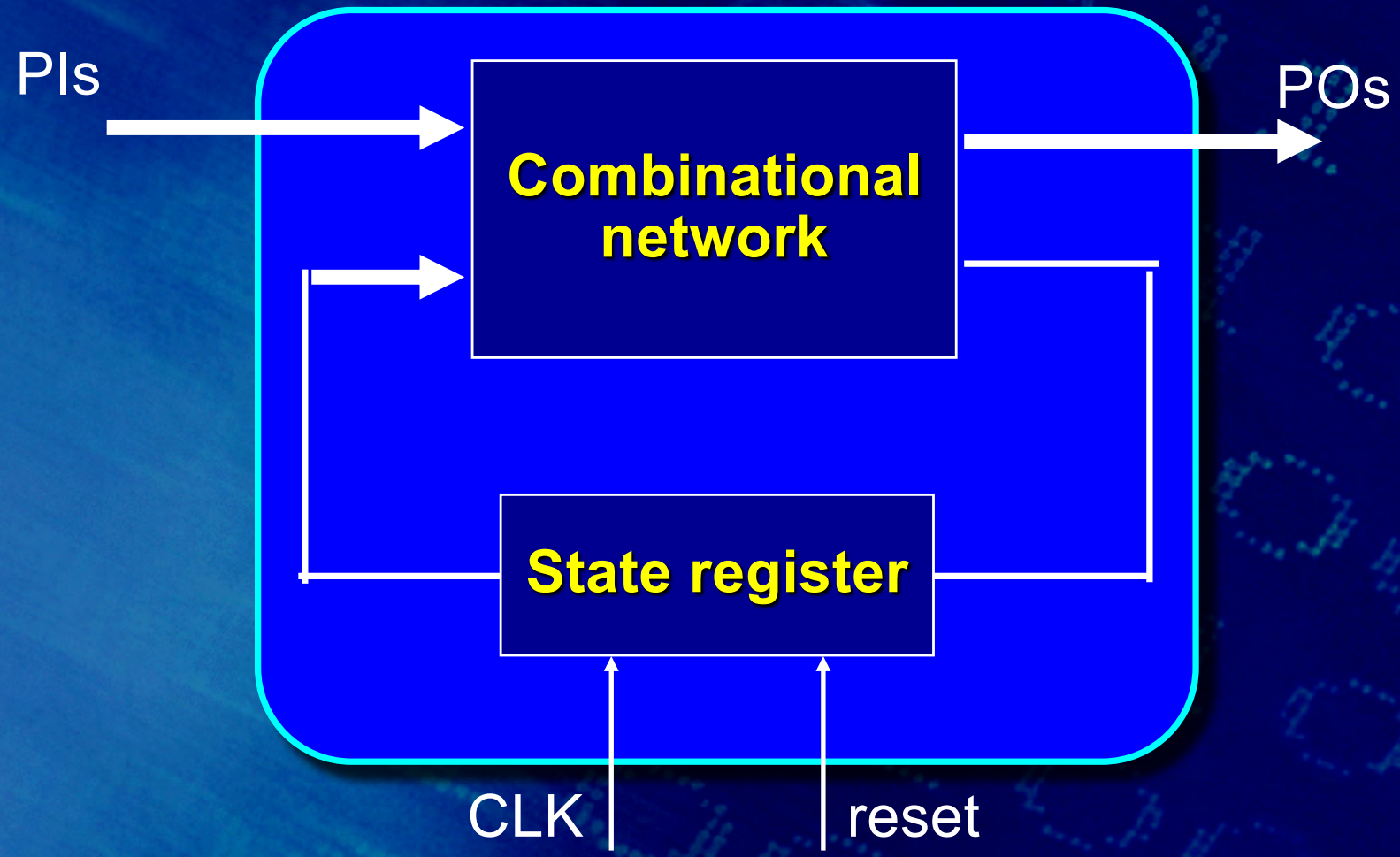
Any FSM, regardless its complexity, MUST have:

- **a particular control input signal, named *reset signal* (or simply *reset*) characterized by the highest priority**
- **a particular state, named *reset state*, in which the network moves whenever the reset signal is asserted.**

Asynchronous reset



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Outline

- Combinational vs. sequential networks
- Moore vs. Mealy machines
- I/O clustering

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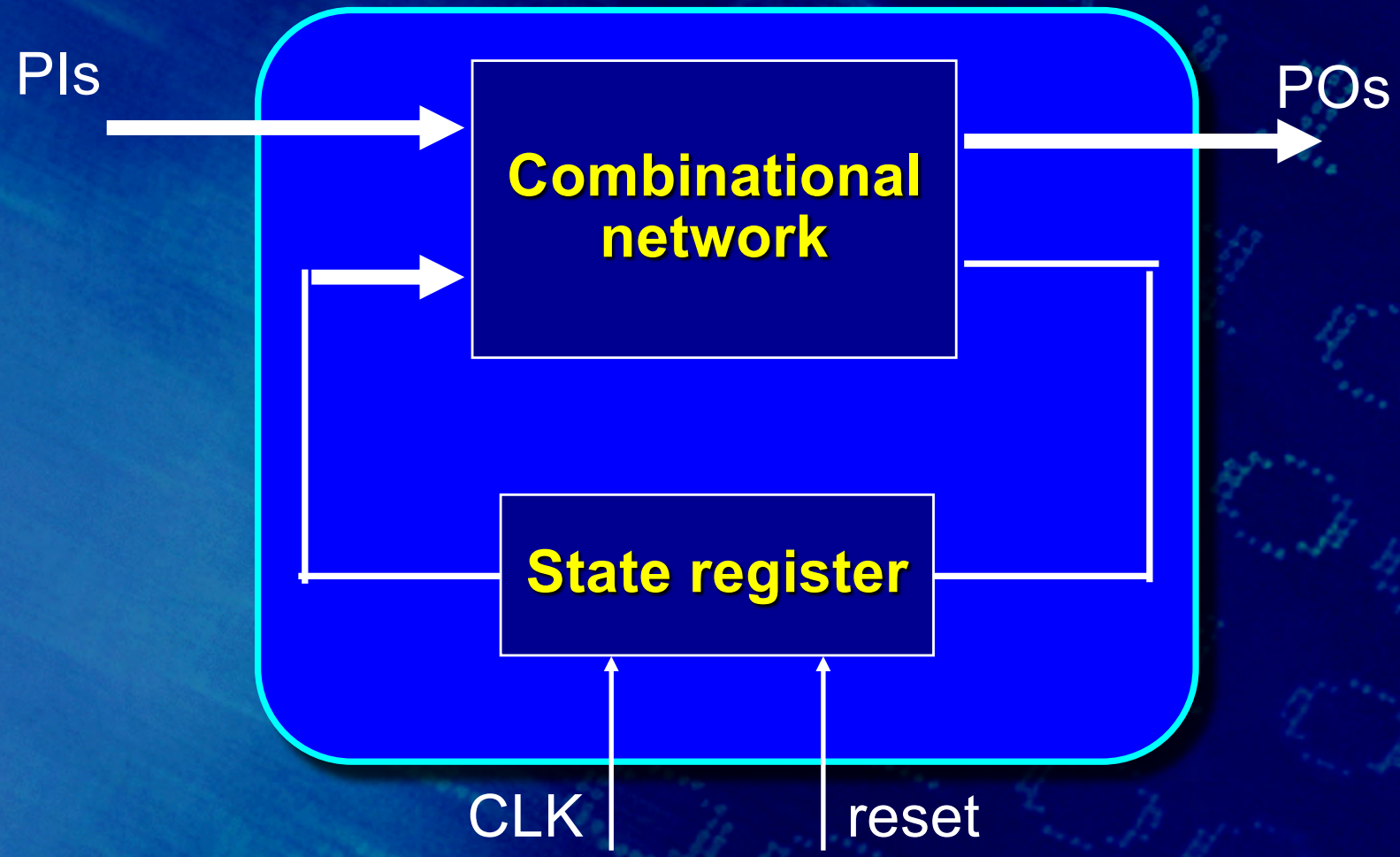
Combinational network splitting



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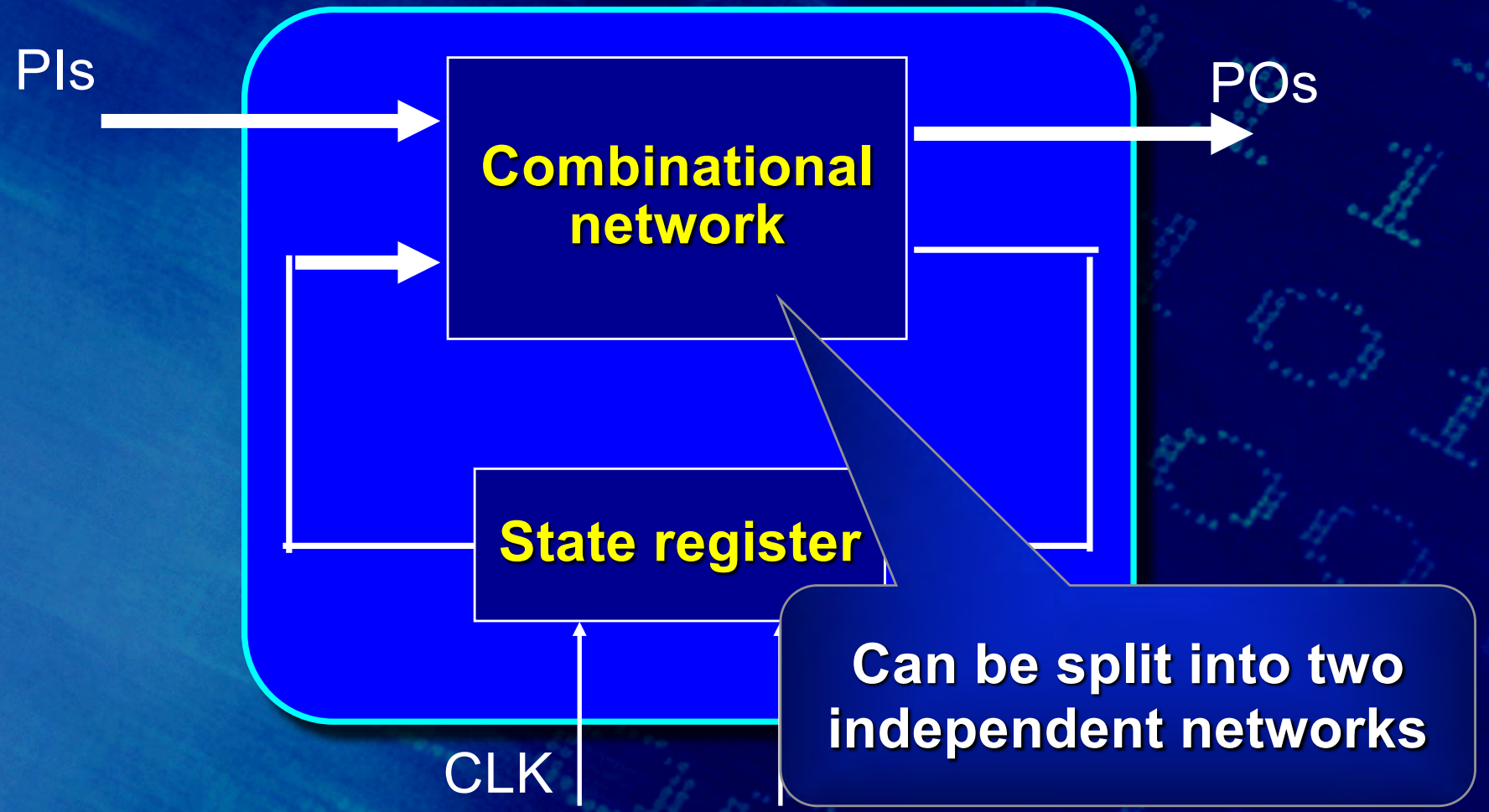
Combinational network splitting



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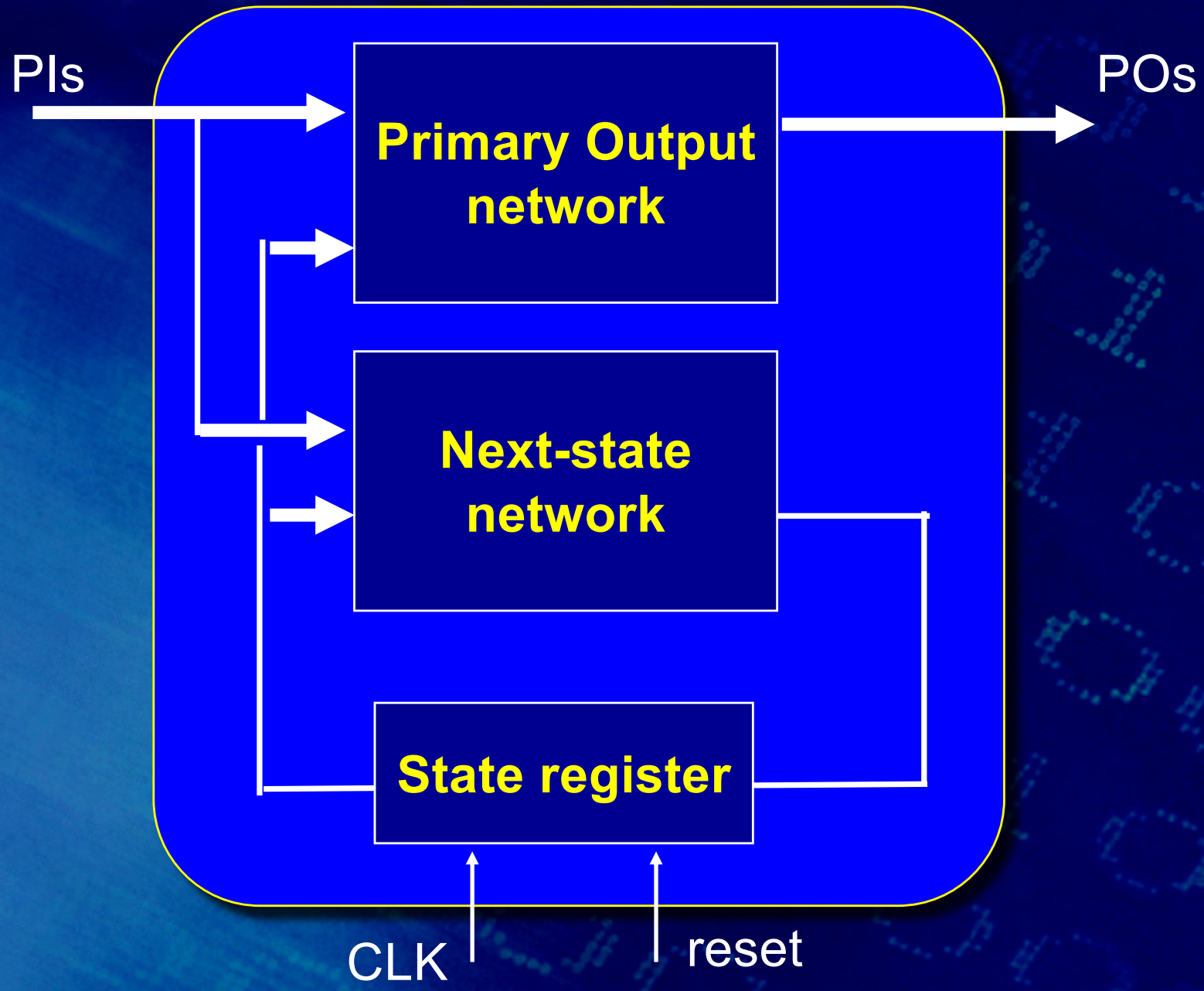

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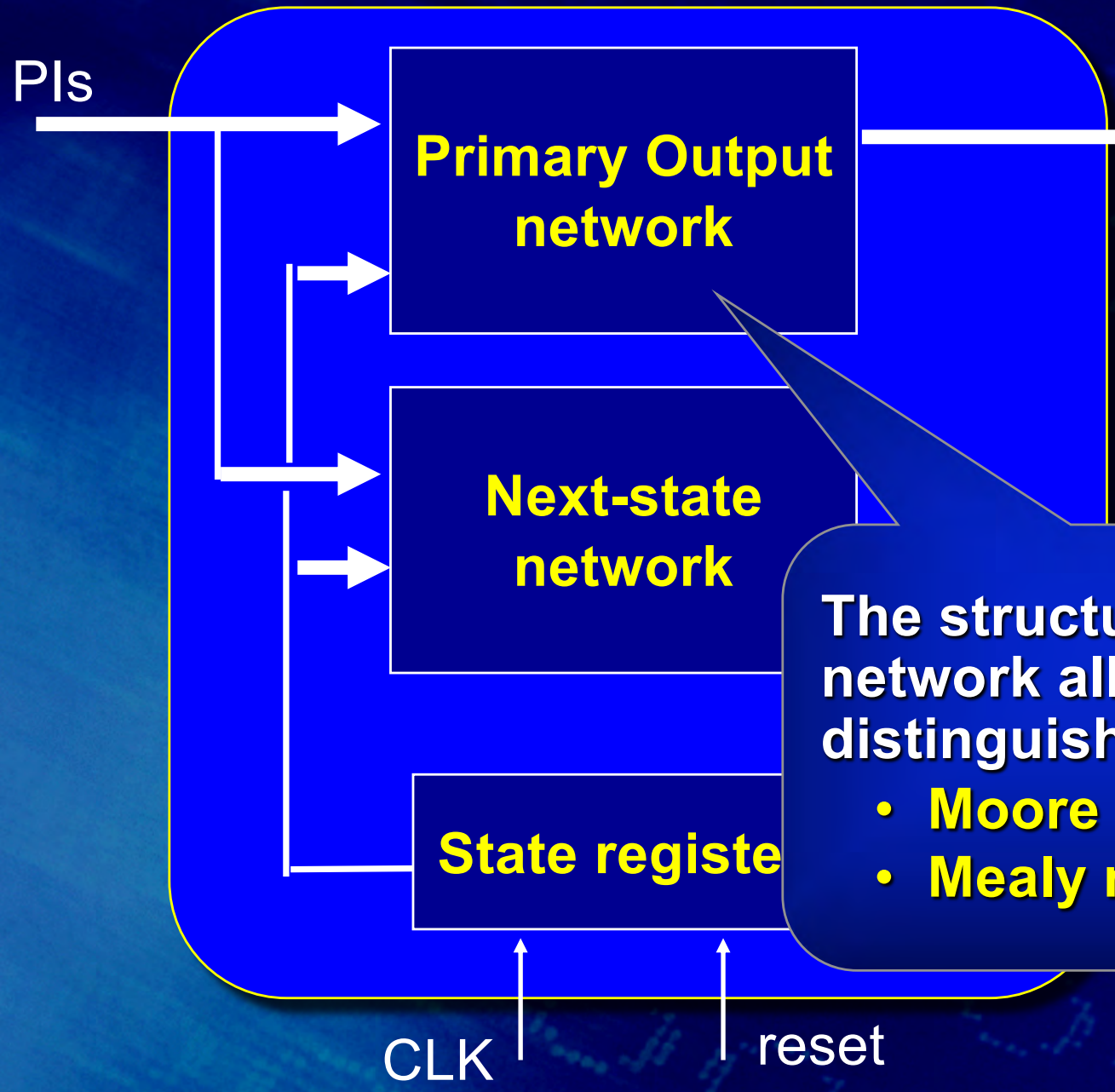

The structure of this network allows us to distinguish between:

- Moore machines
- Mealy machines

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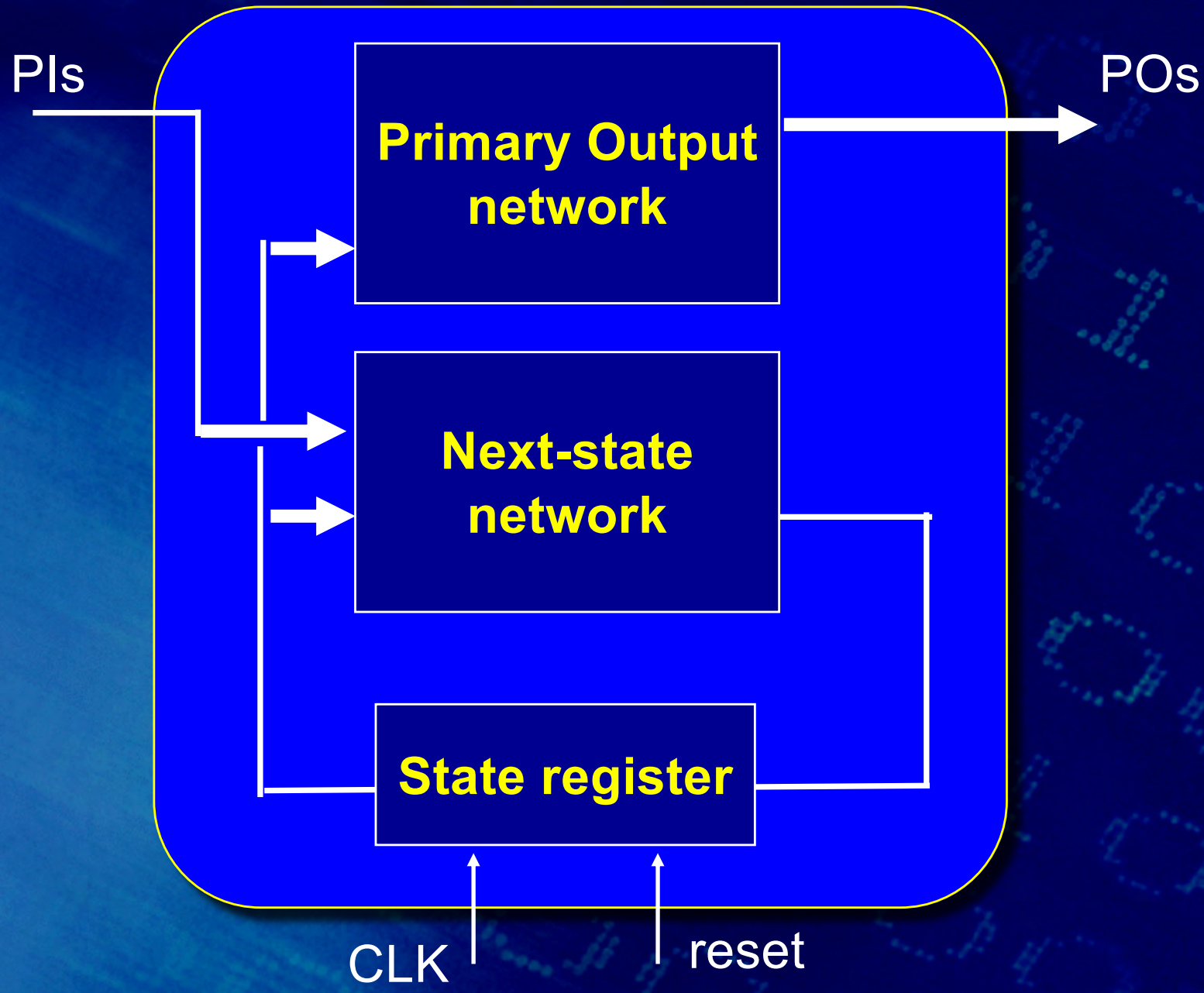
Moore machines

– POs depend on the present state value, only.

POs can change only when state changes.



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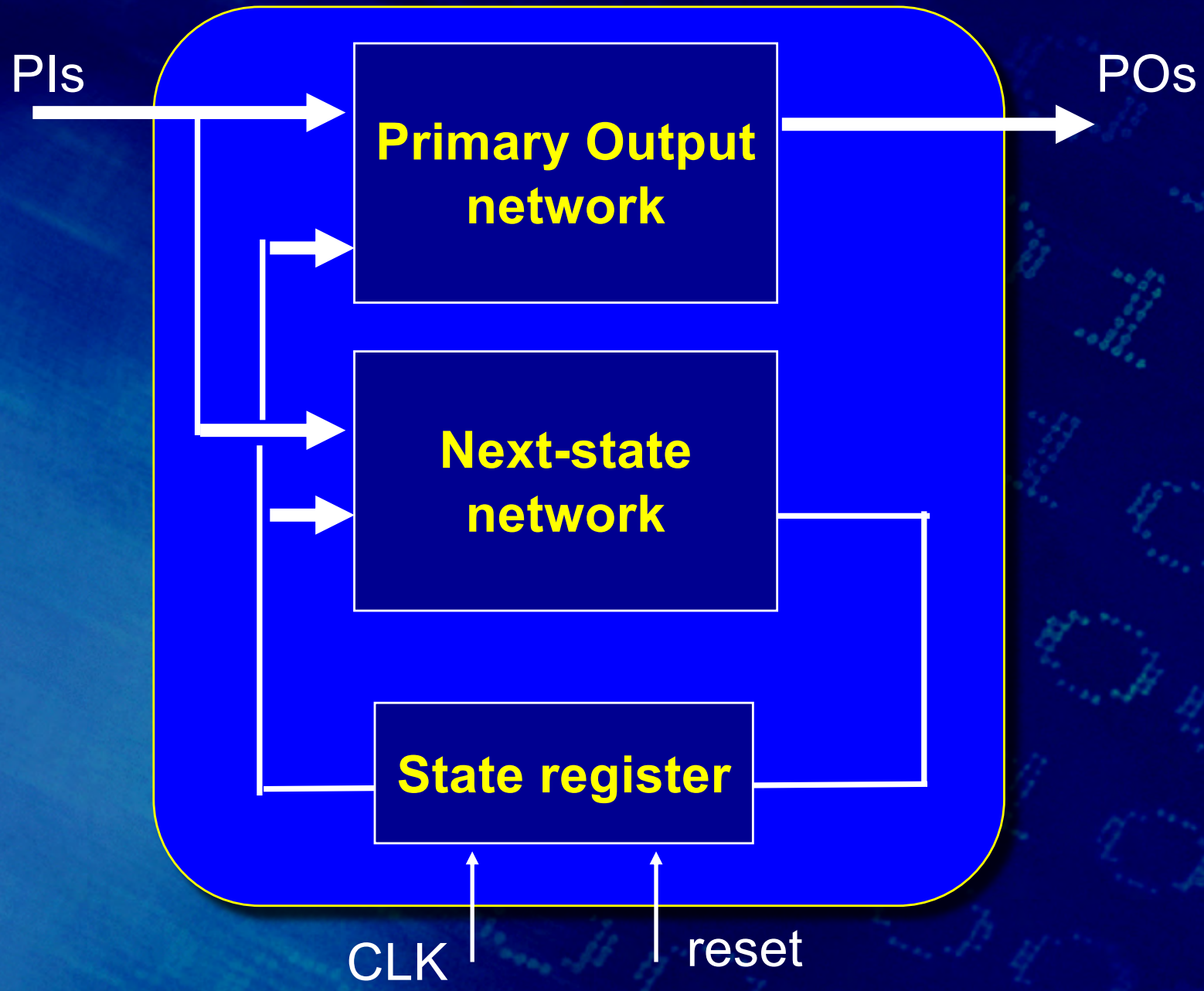
Mealy machines

– POs depend on both the present state value and the PIs values.

POs can change not only when the state changes, but when PIs change, too.



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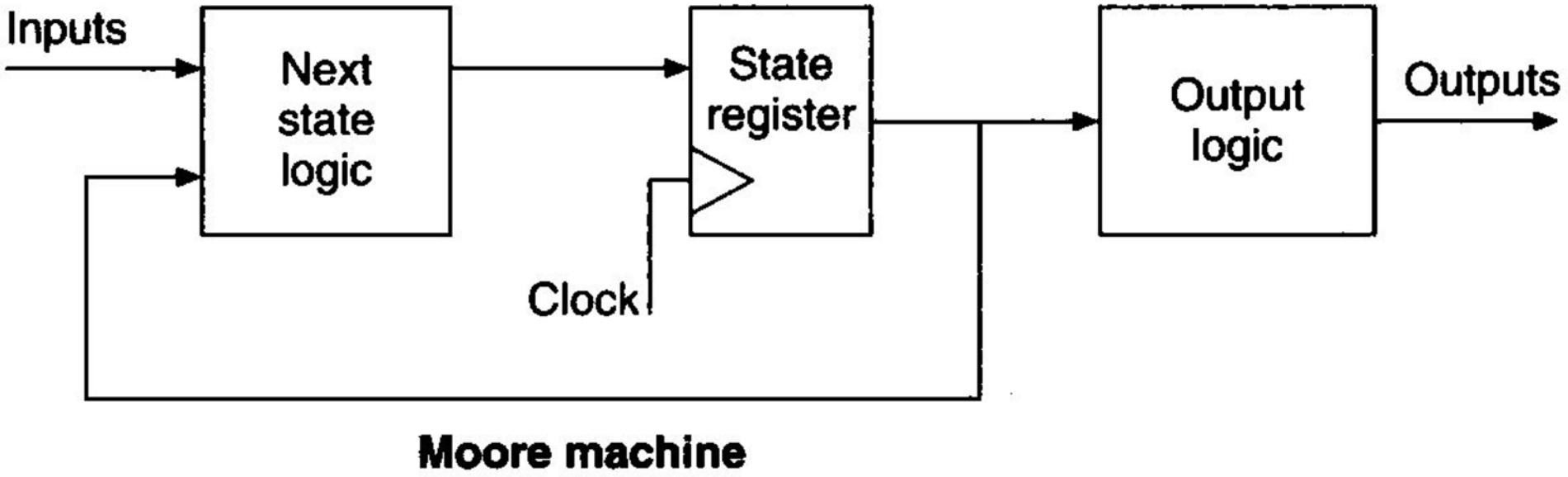
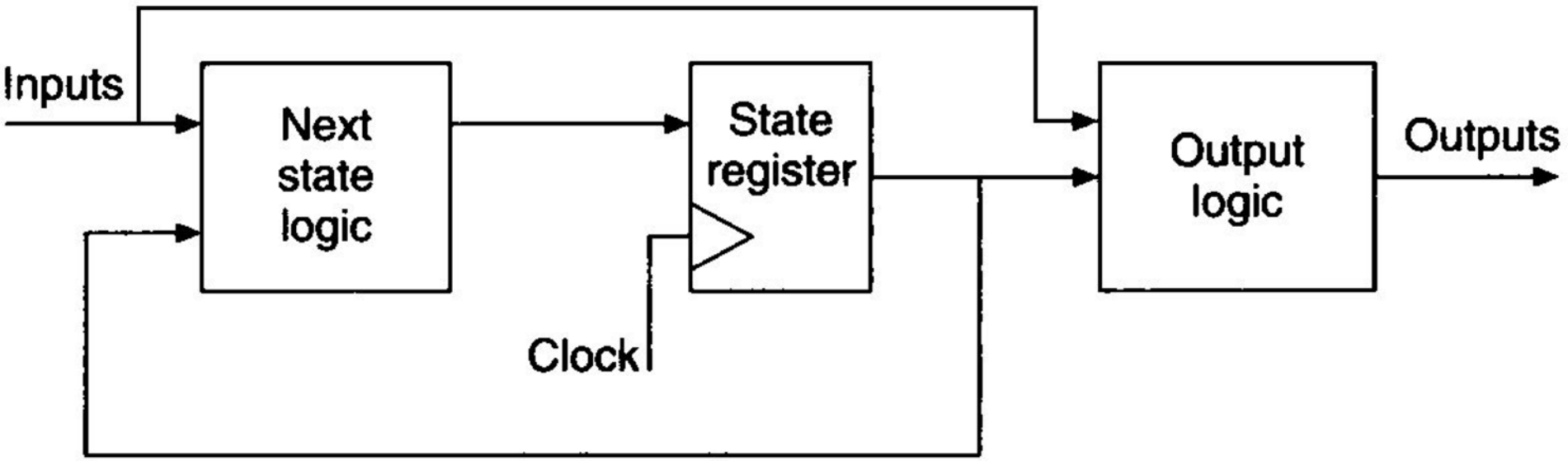


Moore machine



Mealy machine

Outline

- Combinational vs. sequential networks
- Moore vs. Mealy machines
- I/O clustering

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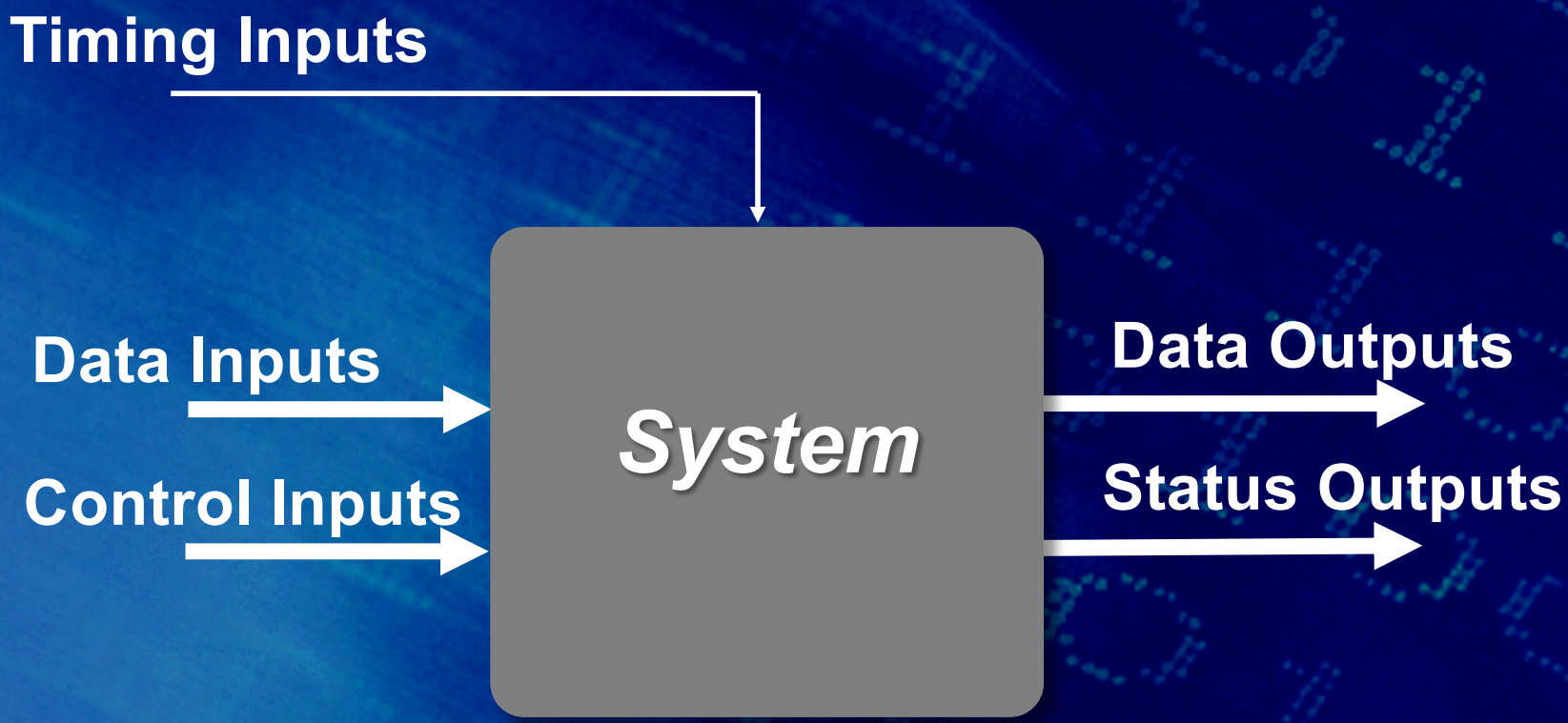
System I/O signals



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Timing Signals

They synchronize the overall behavior of the network by:
sampling data and control inputs
updating data and control outputs

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Edge vs. pulse triggering

- Sampling and updating can be triggered by
  - clock's raising or falling edges
  - clock's positive or negative pulses.

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Edge triggering behavior

- **The same clock edge samples the inputs and concurrently updates the outputs:**
  - **raising edge → *positive edge triggered***
  - **falling edge → *negative edge triggered***

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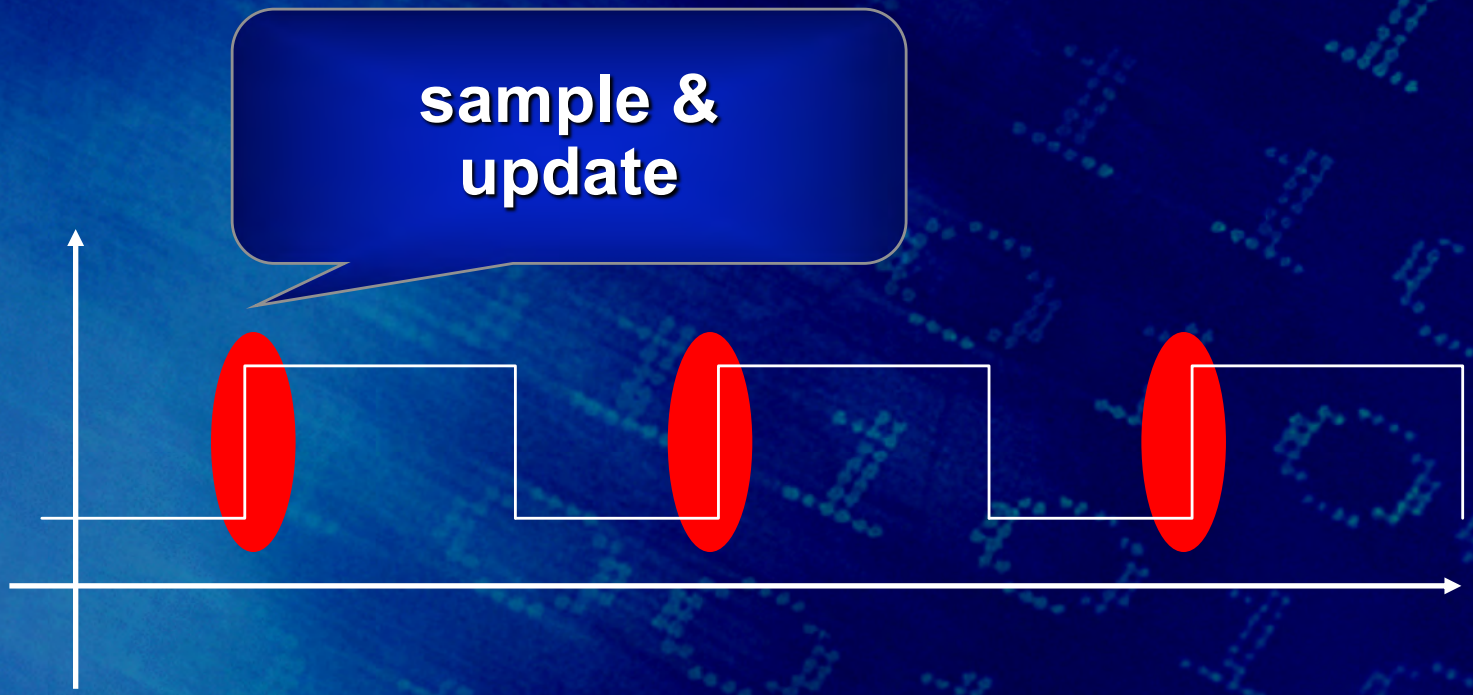
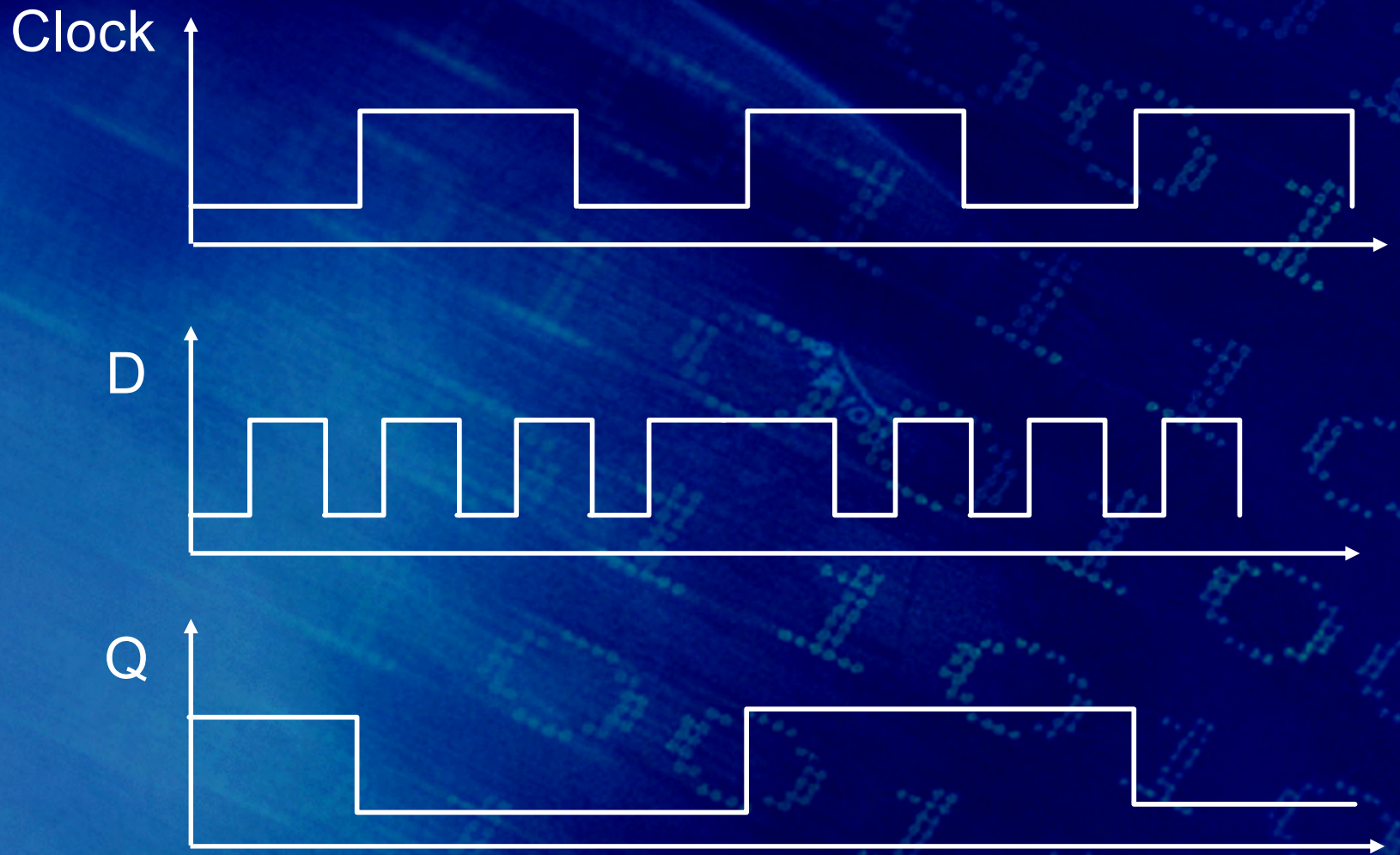
Positive edge triggered



Positive edge triggered



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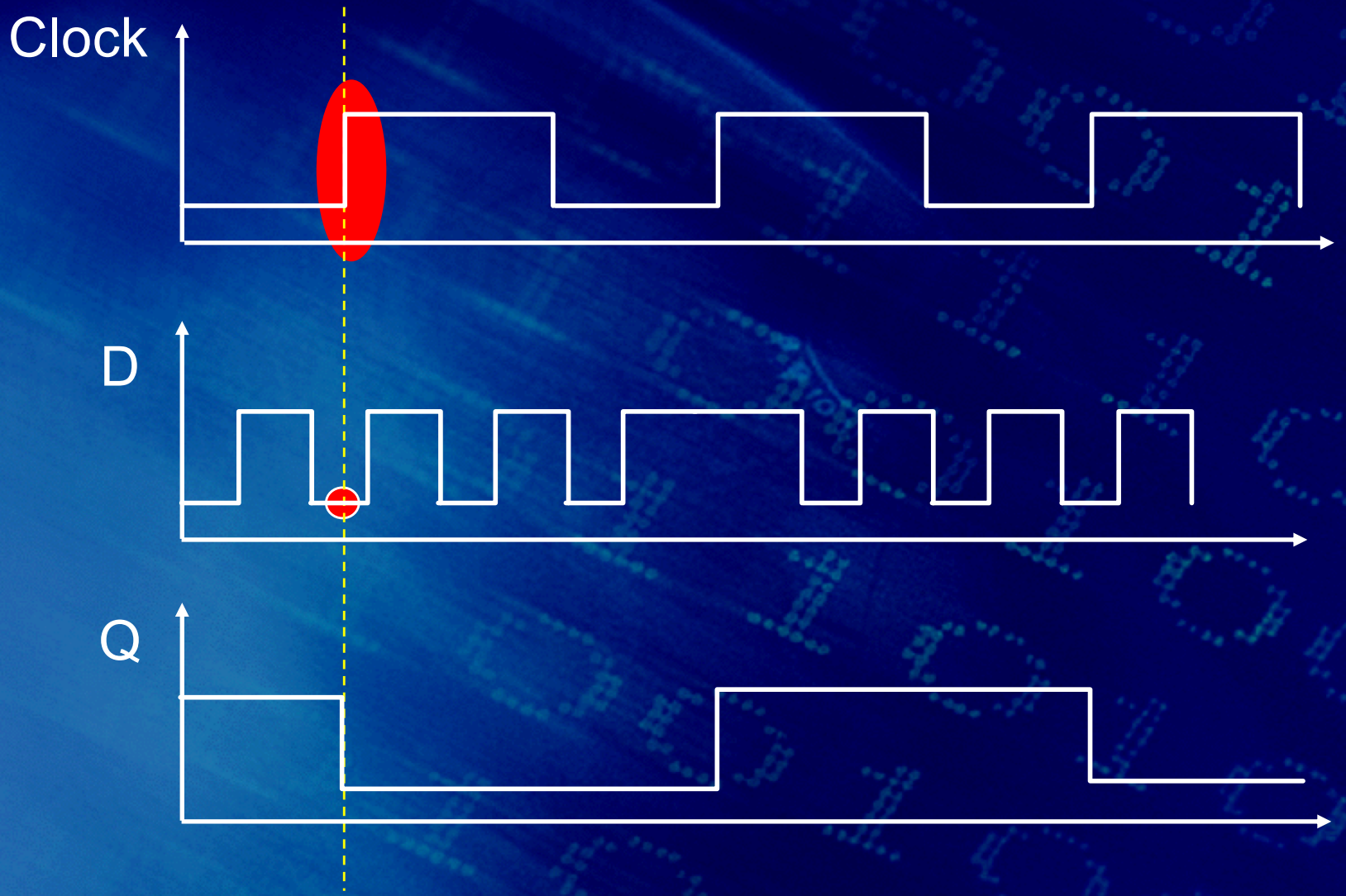
Positive edge triggered



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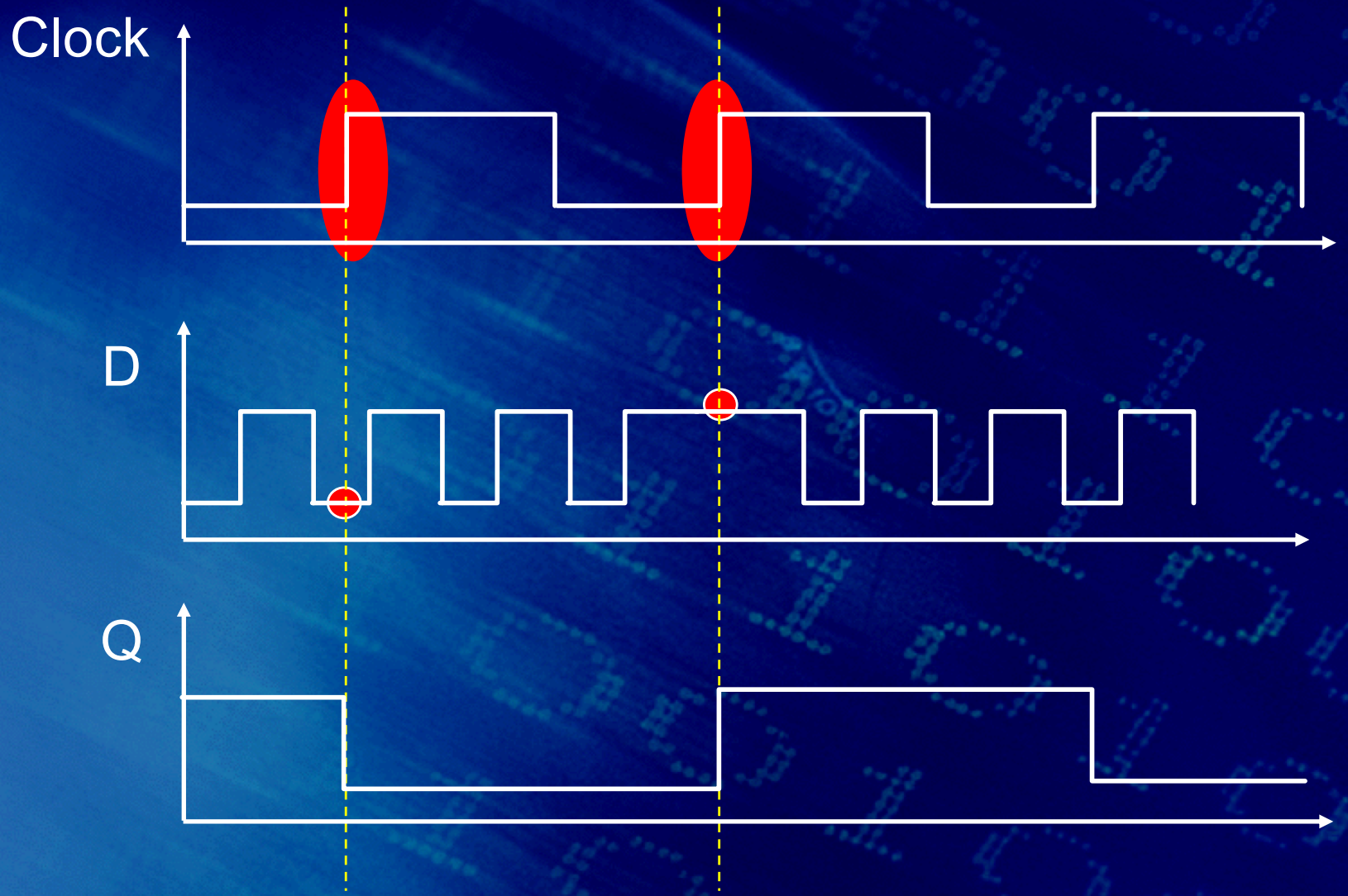
Positive edge triggered



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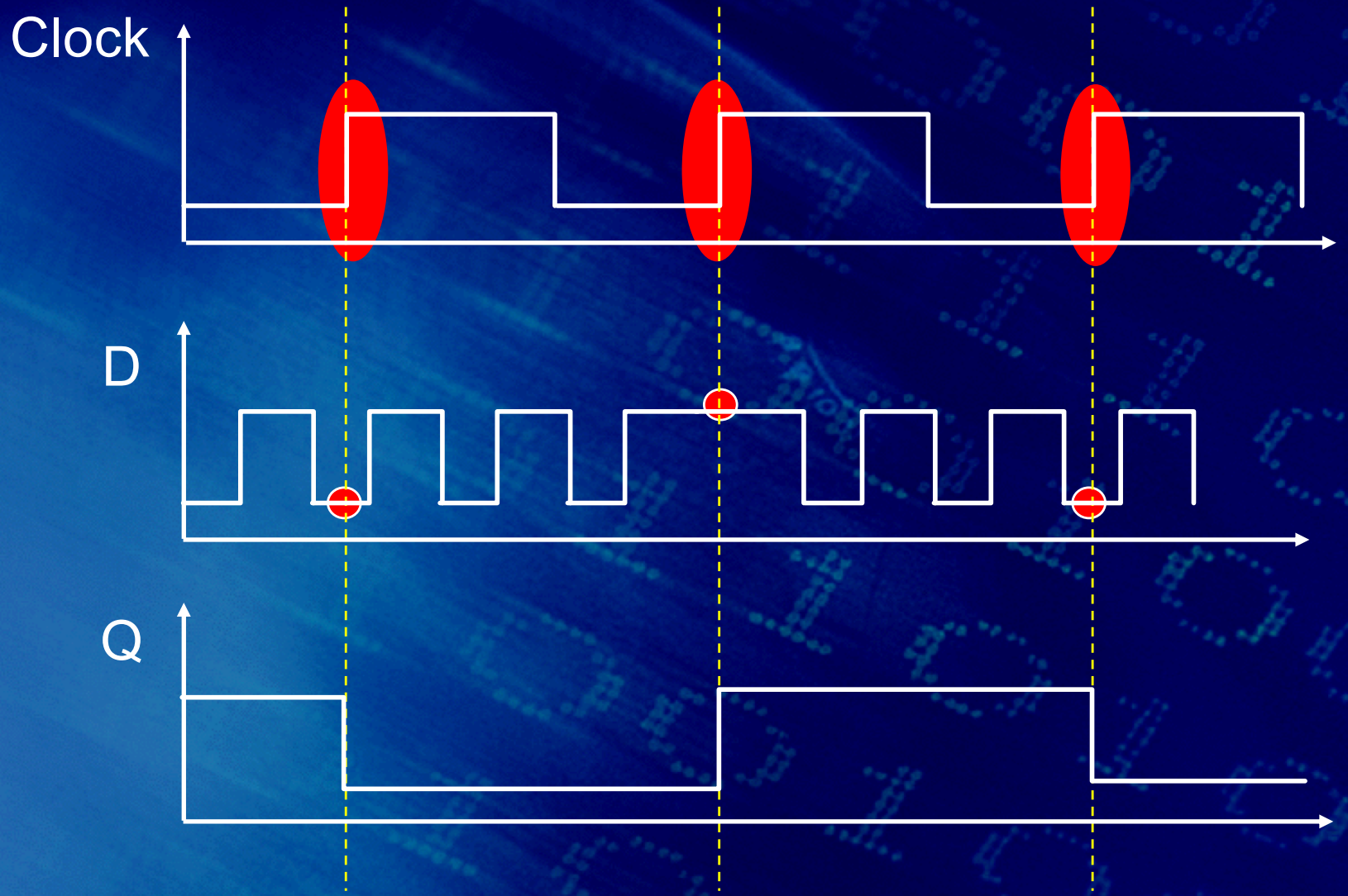
Positive edge triggered



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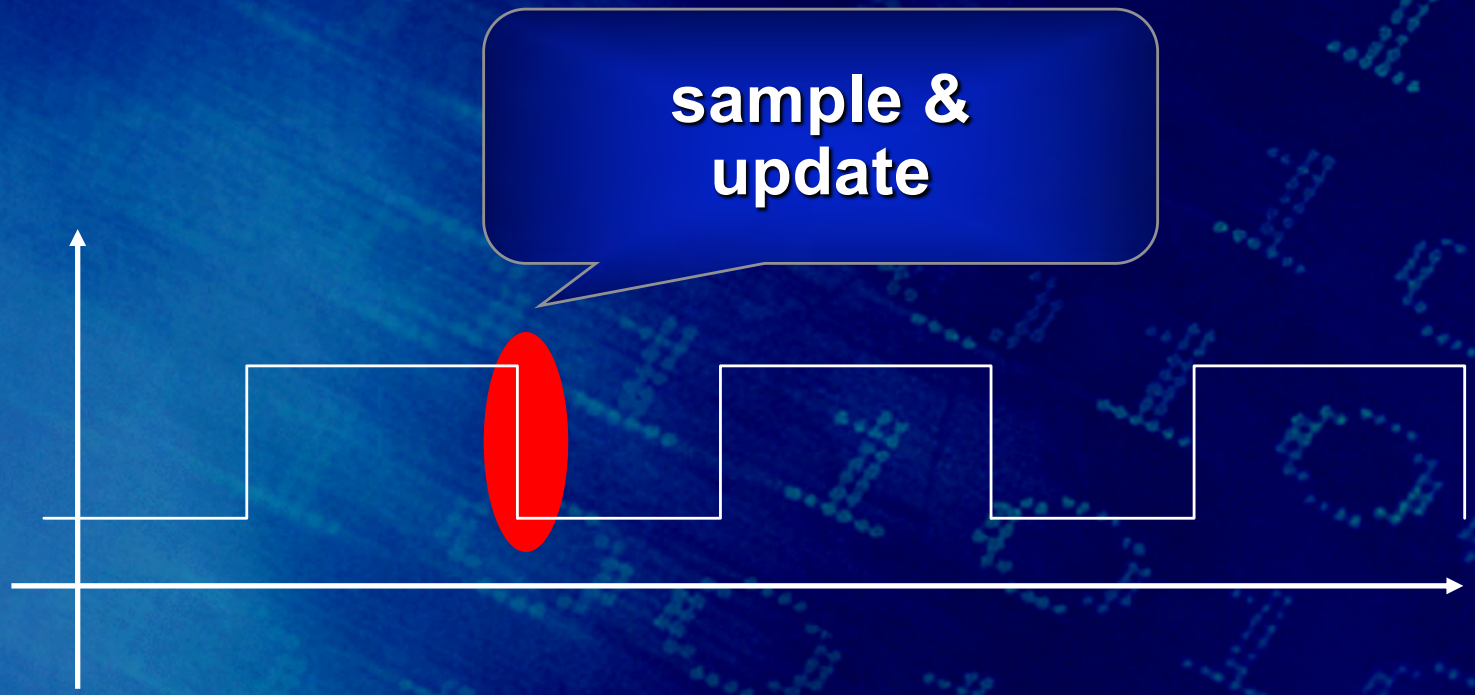
Negative edge triggered



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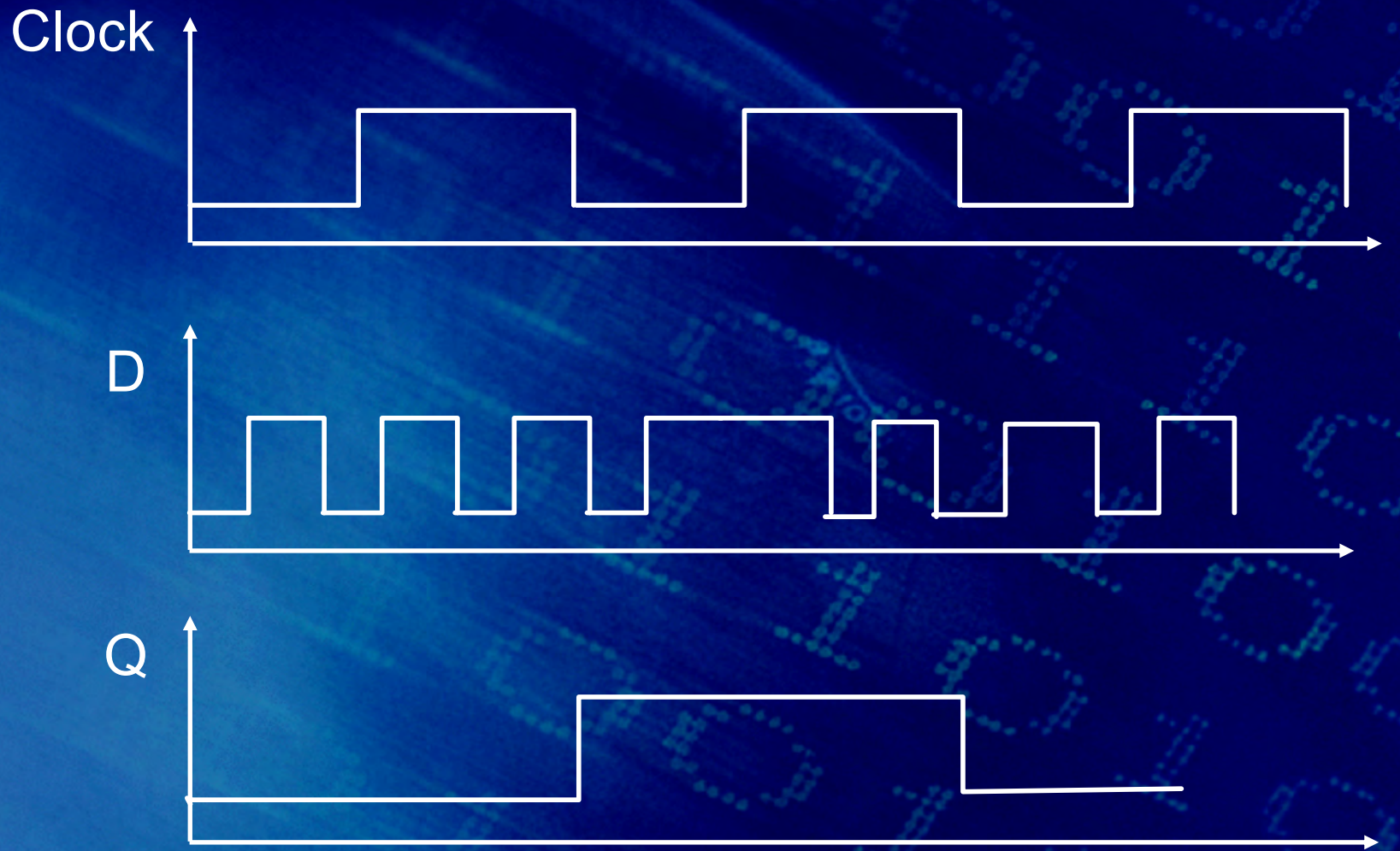
Negative edge triggered



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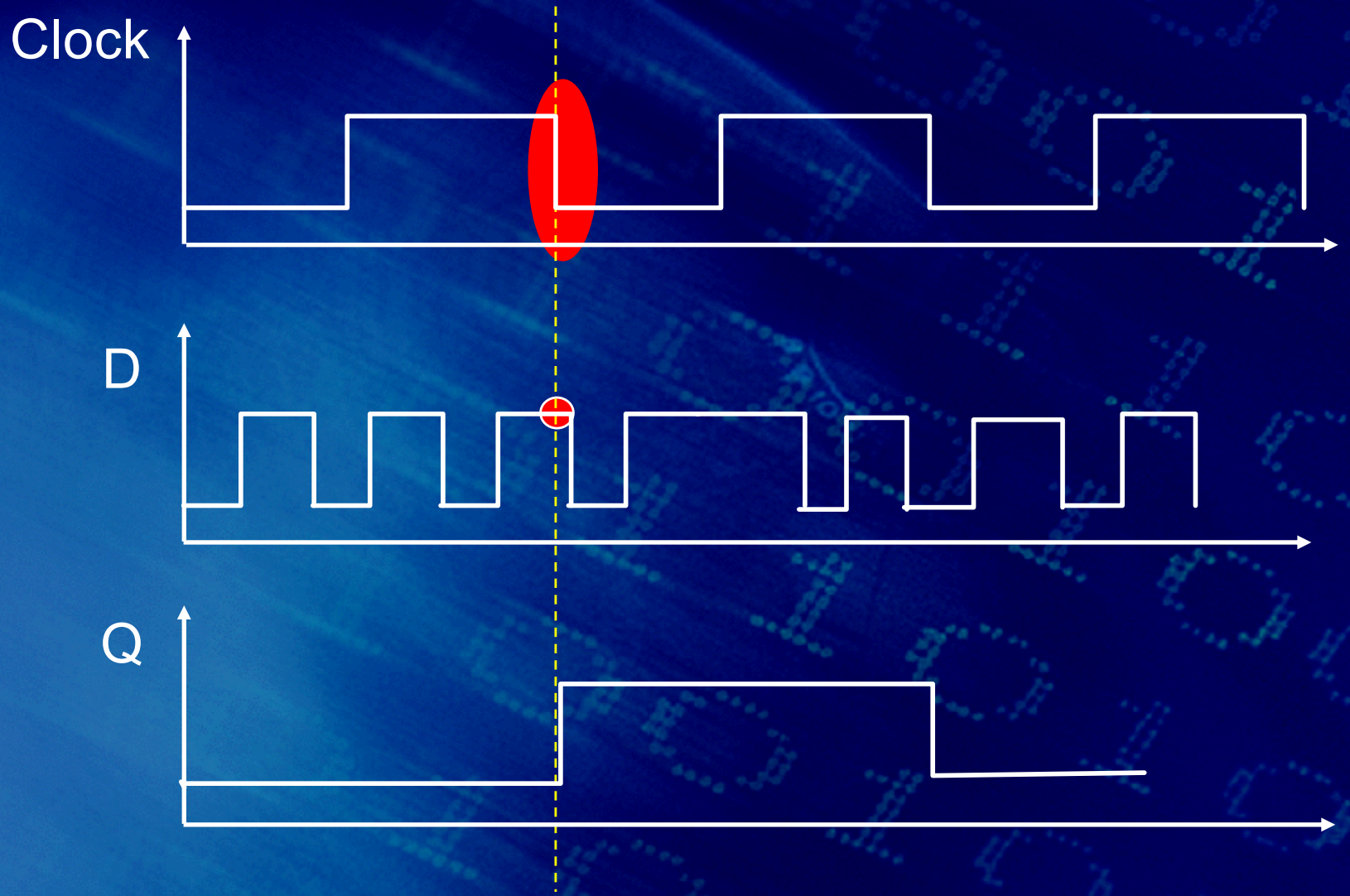
Negative edge triggered



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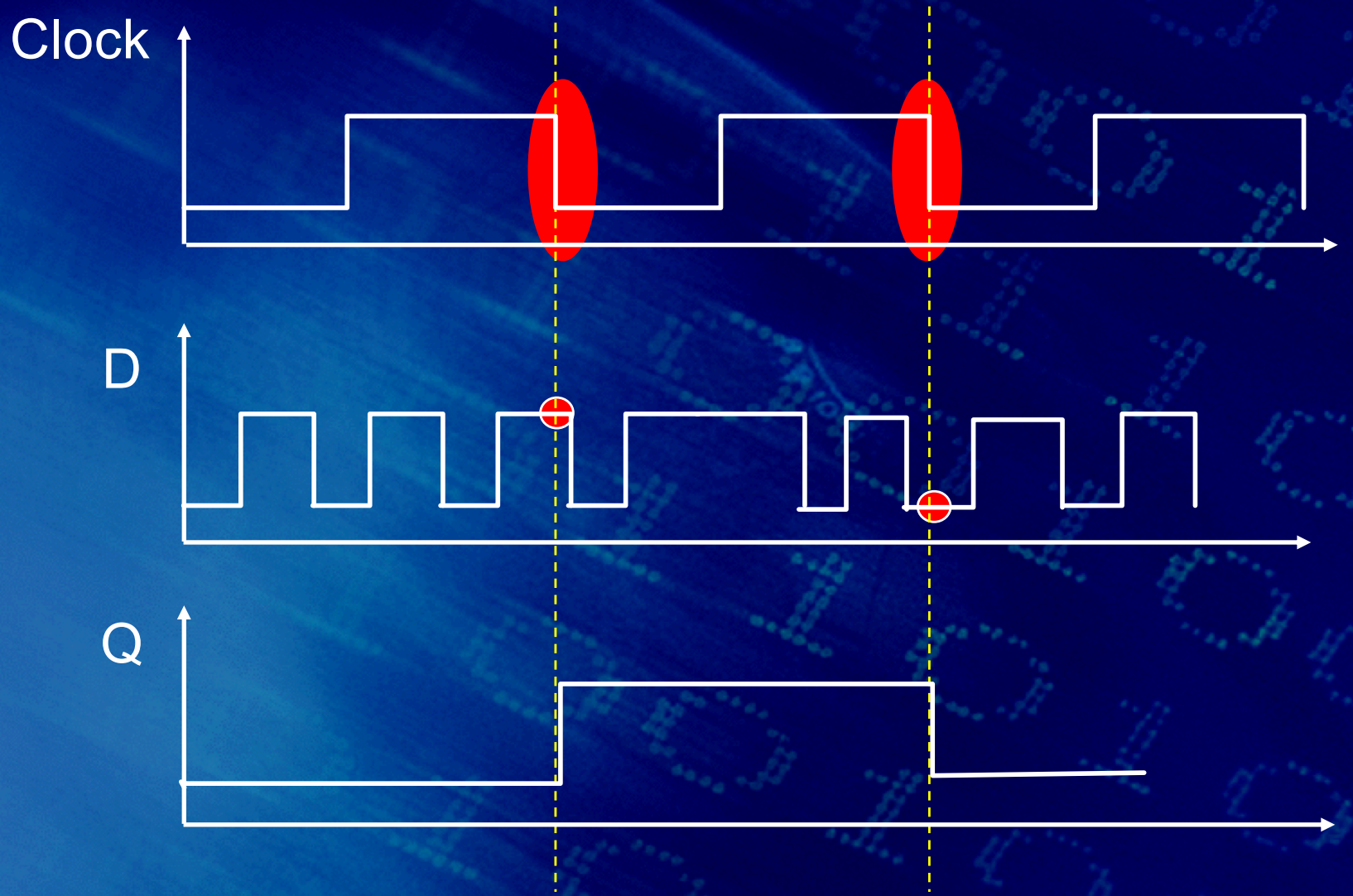
Negative edge triggered



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Pulse triggering behavior

- **An edge of the clock samples the inputs values and the other edge updates the outputs**

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Positive pulse triggered

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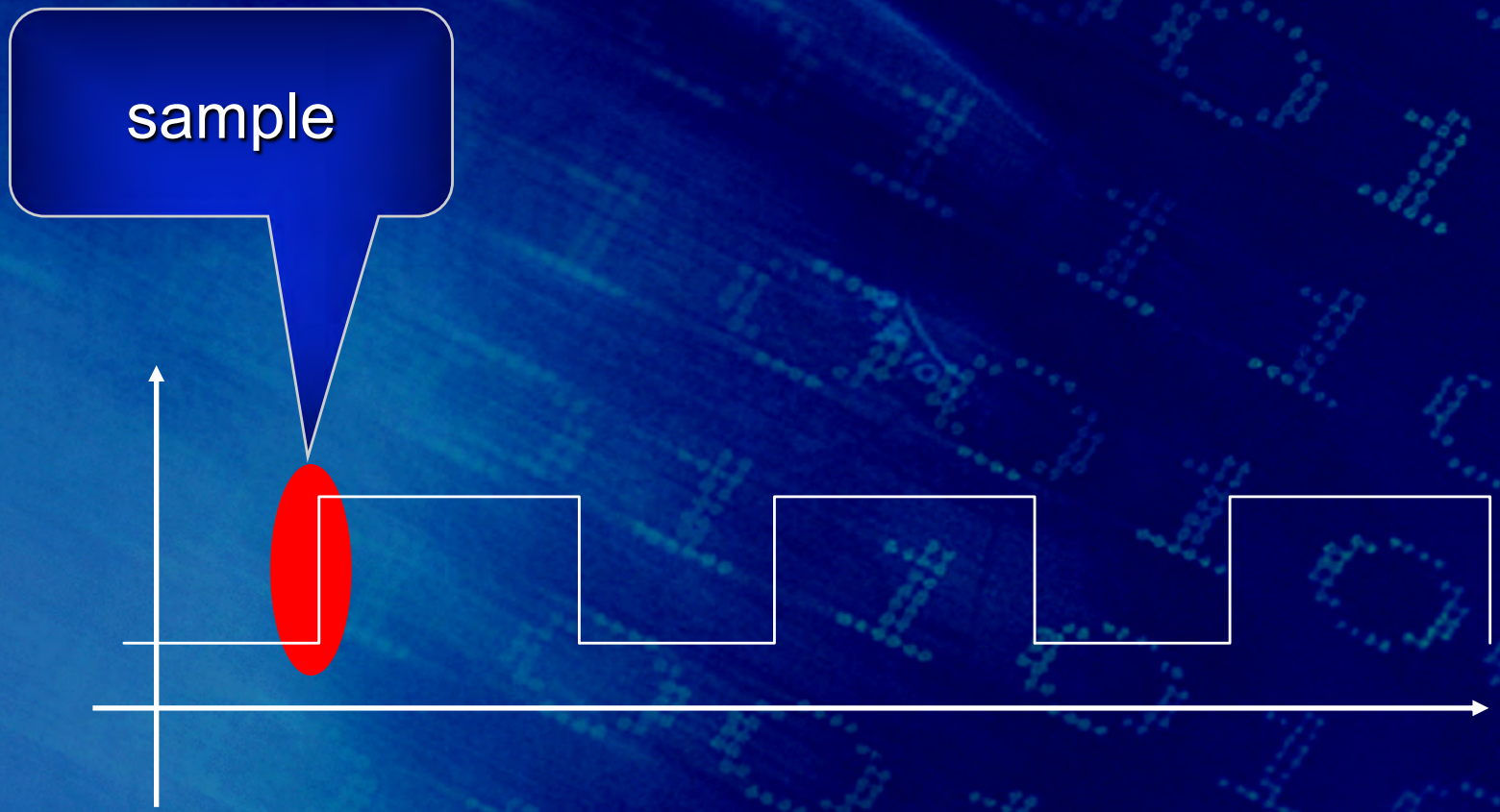
Positive pulse triggered



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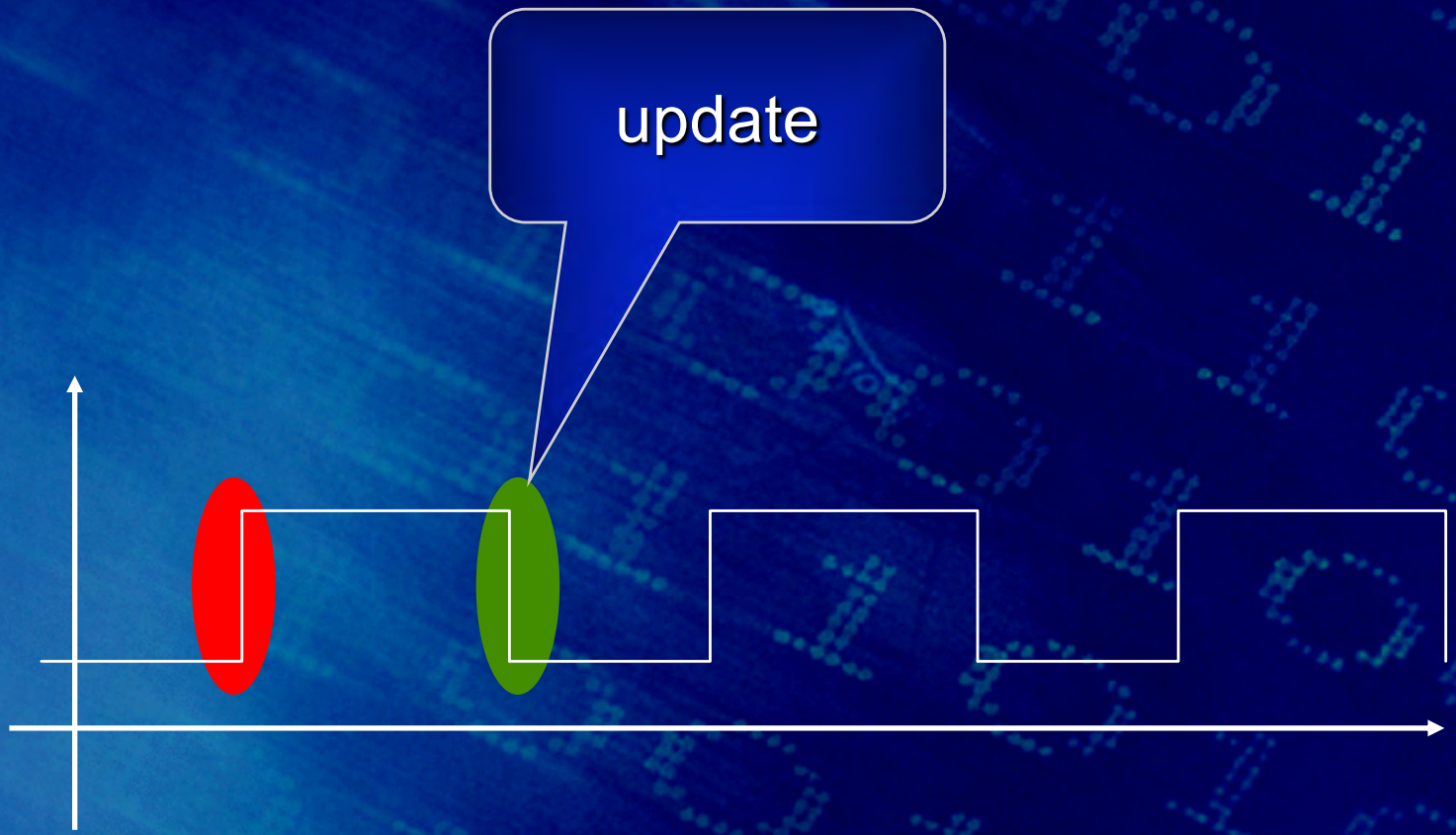
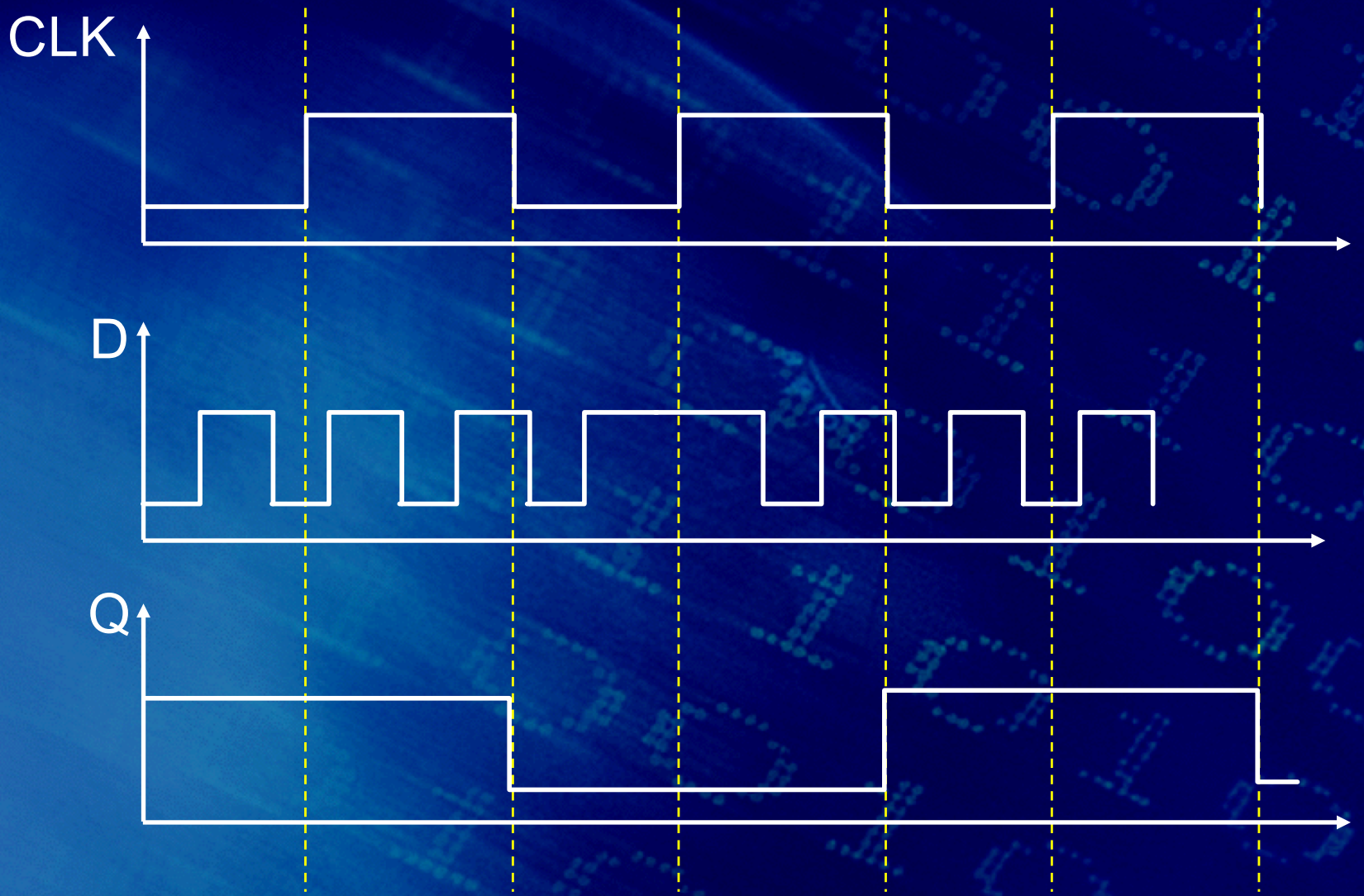
Positive pulse triggered

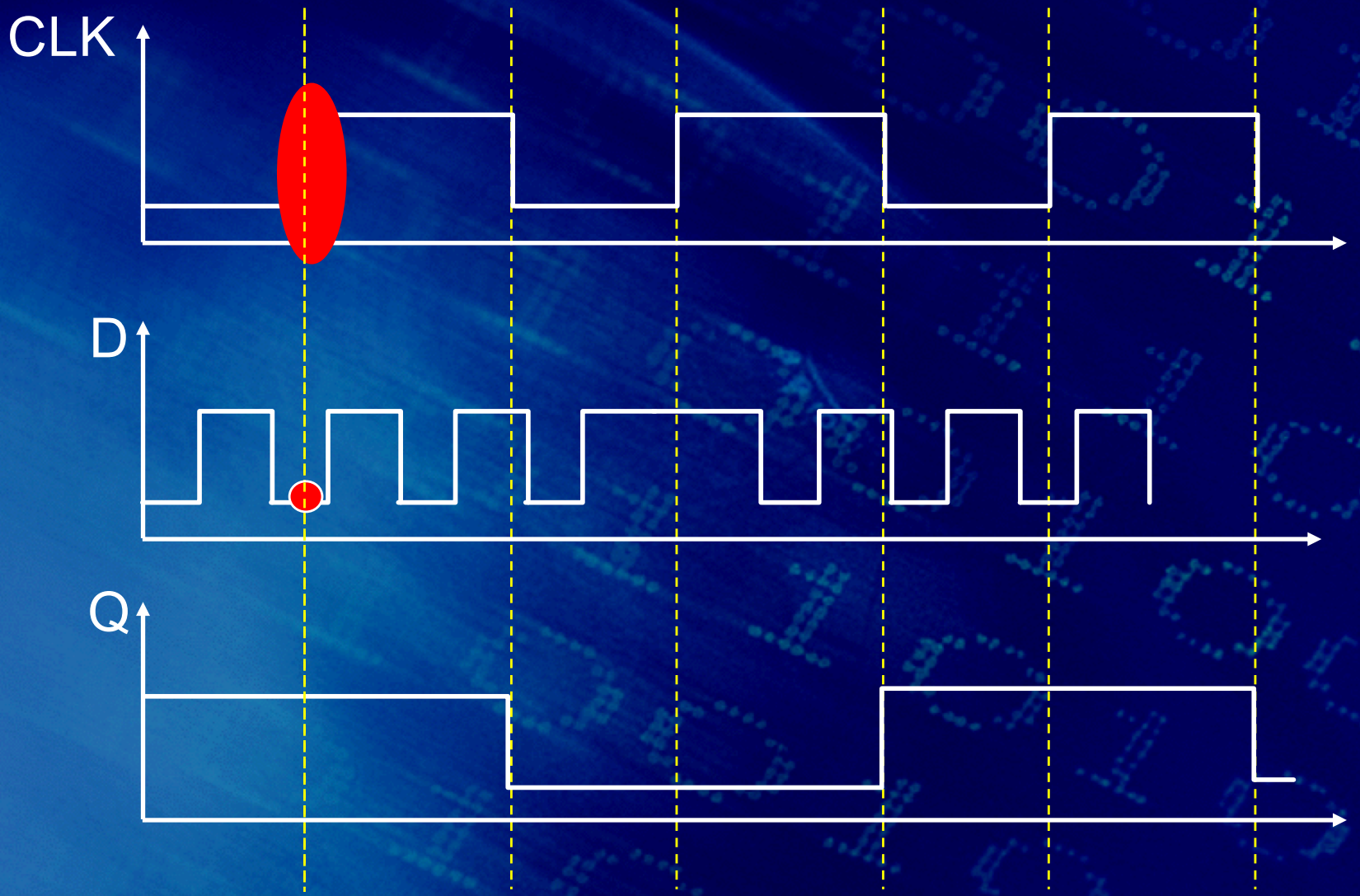


Positive pulse triggered



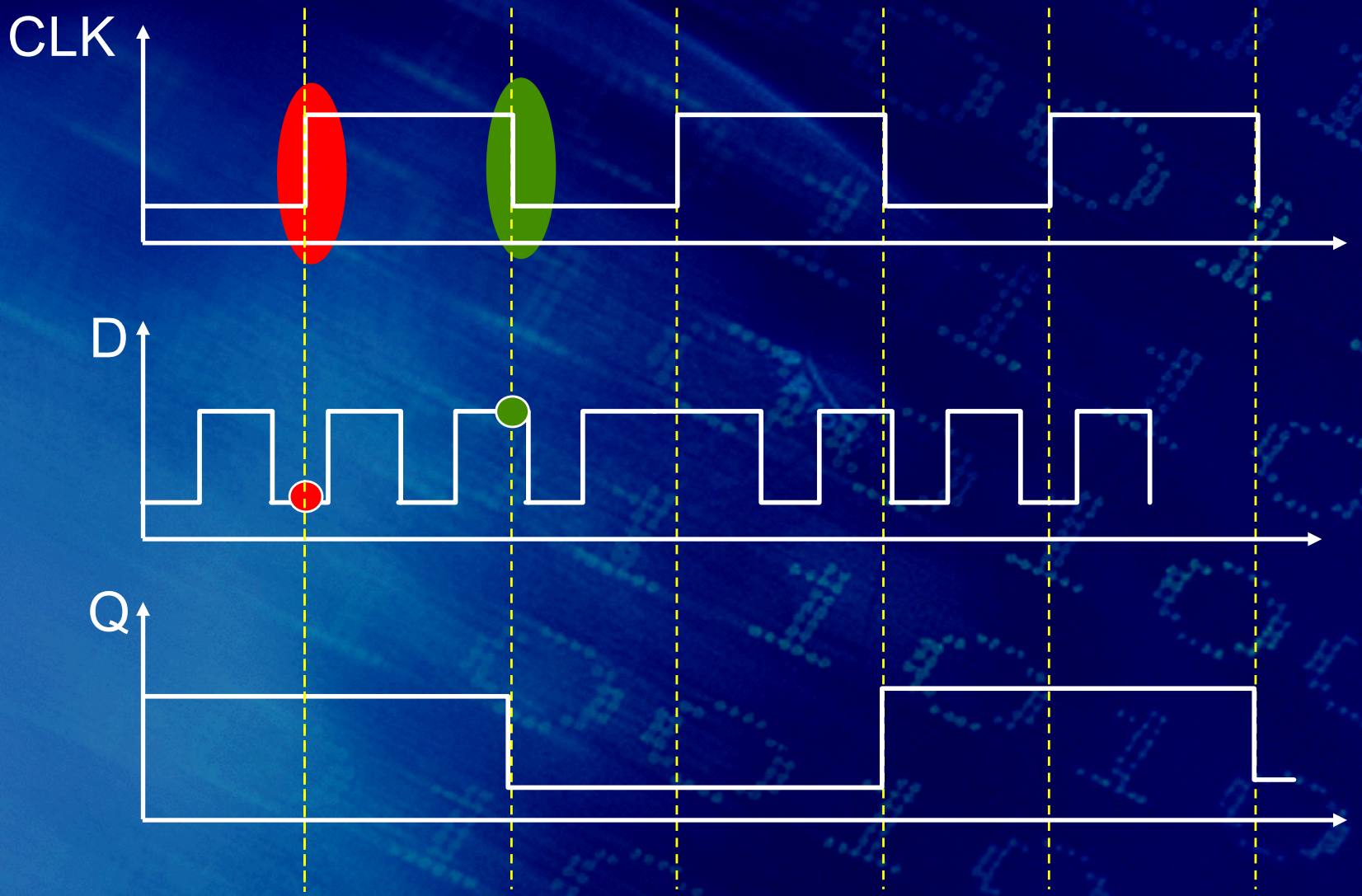
Rel. 12.03.2019

Positive pulse triggered



Rel. 12.03.2019

Positive pulse triggered



Rel. 12.03.2019

Set-up & Hold Times

- **Sequential devices works properly iff some temporal constraints are satisfied**

Rel. 12.03.2019

Set-up time

The time interval t_s in which data inputs and control inputs must be stable before the clock event

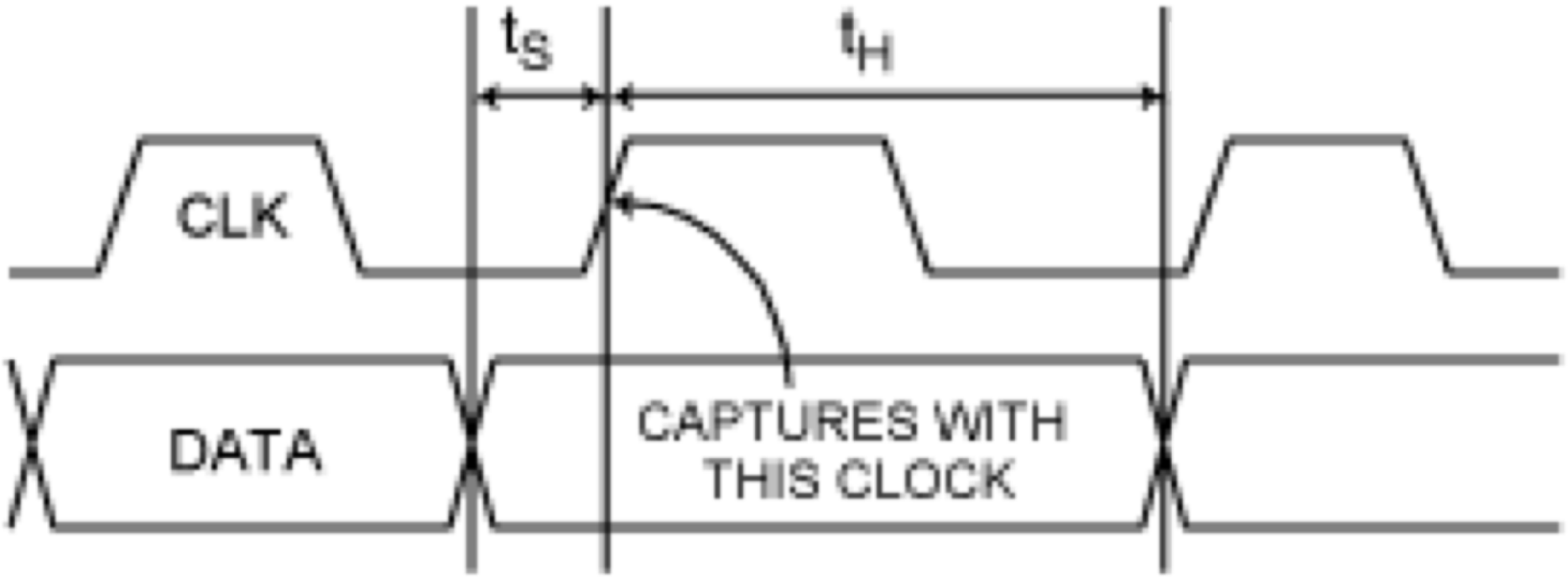
Rel. 12.03.2019

Hold time

The time interval t_h in which data inputs and control inputs must be stable after the clock event

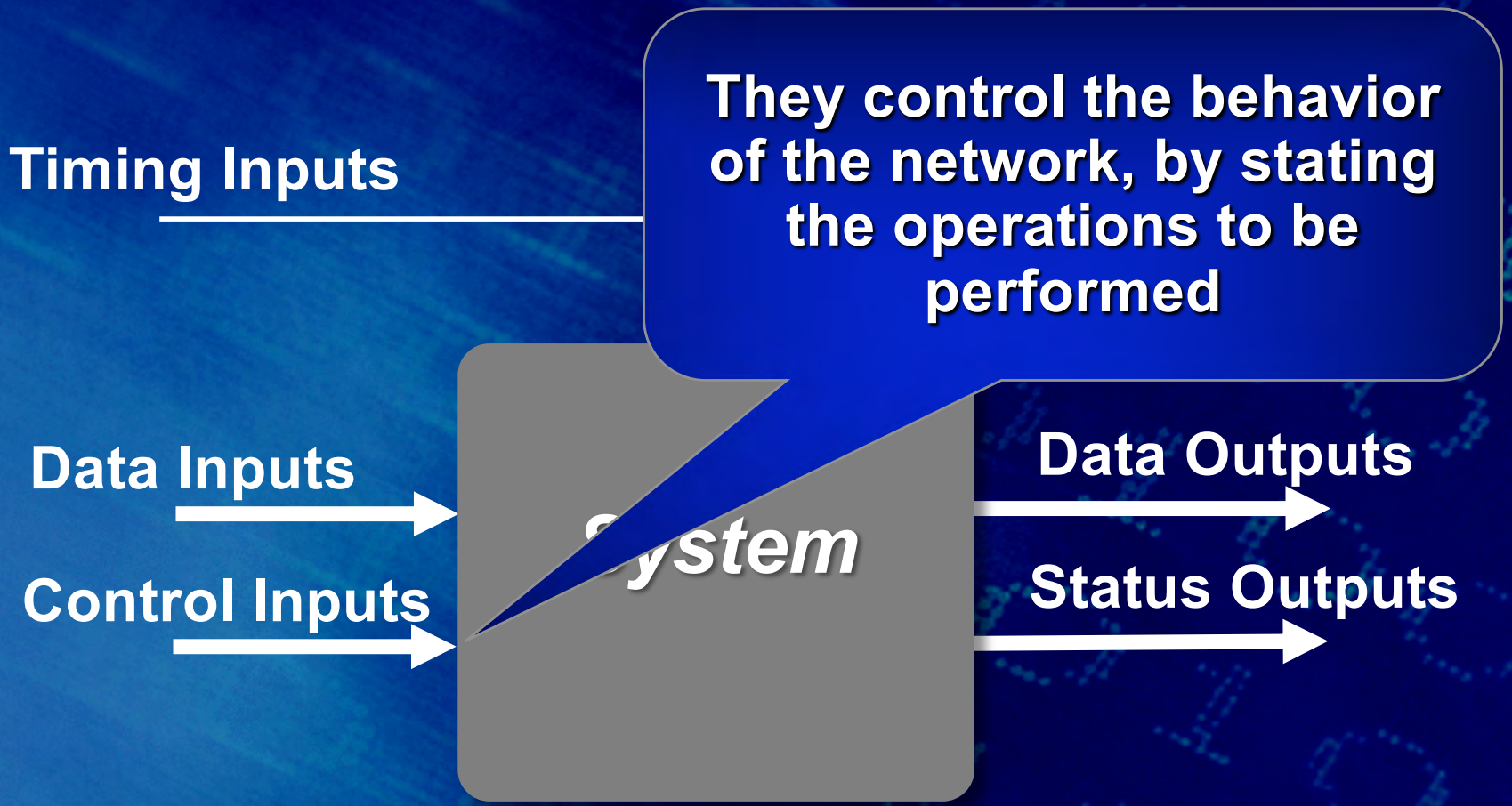
Rel. 12.03.2019

Set-up & Hold Times



Rel. 12.03.2019

Control Signals



Rel. 12.03.2019

Control Inputs classification

- **According to their asserting characteristics, Control Inputs are usually classified as:**
  - ***Synchronous***
  - ***Asynchronous***

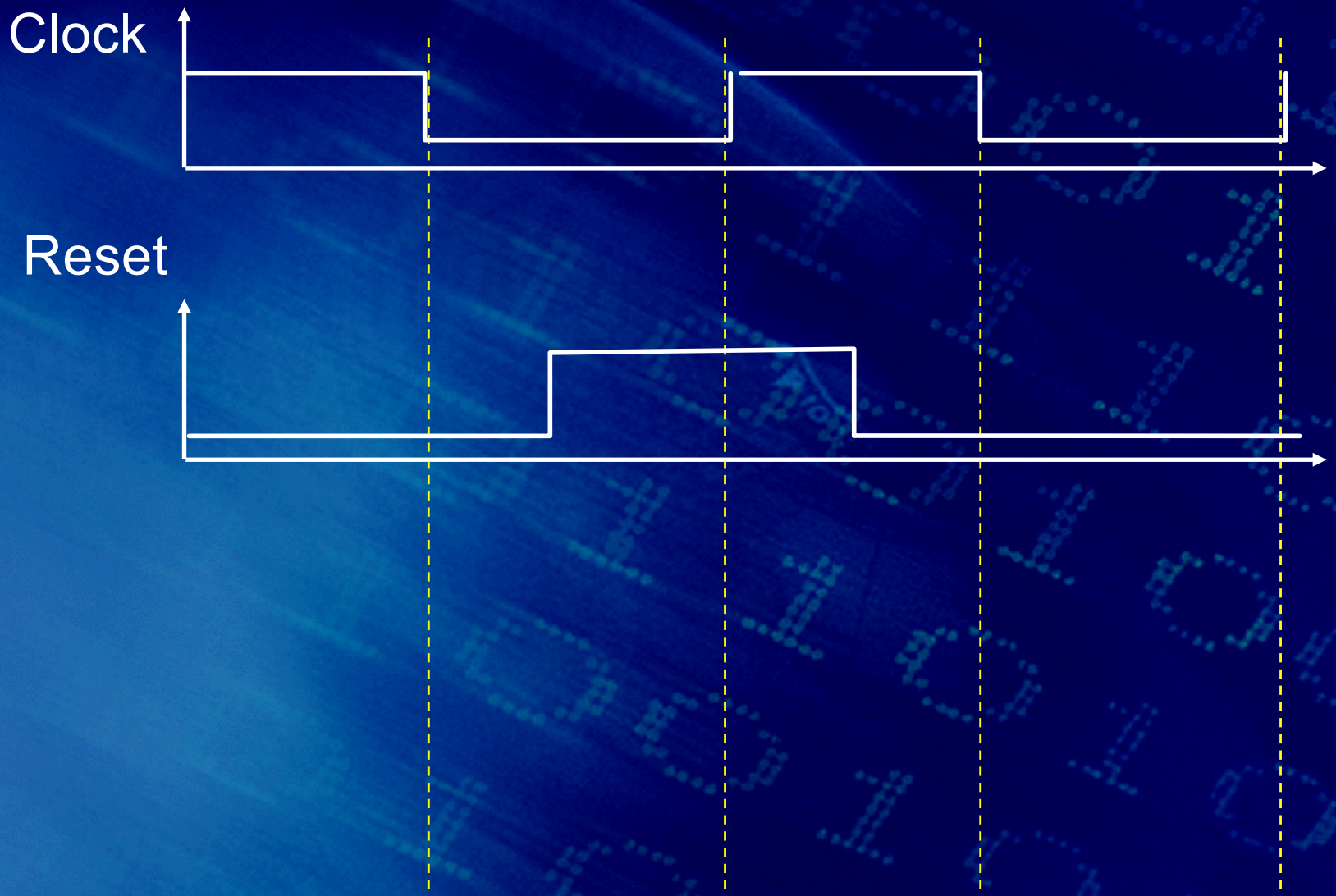
Rel. 12.03.2019

Control Inputs classification

- **According to their asserting characteristics, Control Inputs are usually classified as:**
  - ***Synchronous***
  - ***Asynchronous***

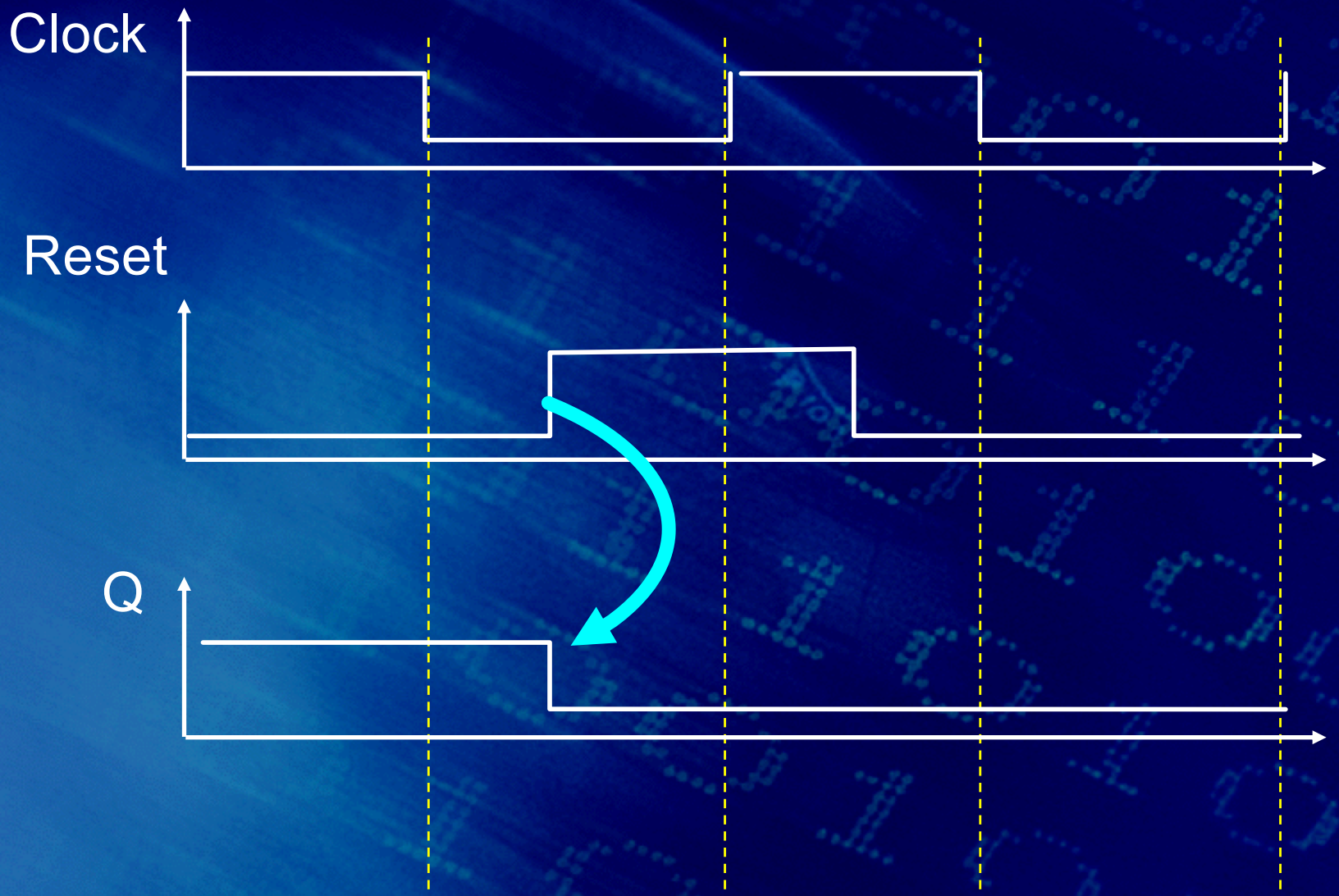
When asserted, they are immediately active, regardless the clock.

Asynchronous reset



Rel. 12.03.2019

Asynchronous reset



Rel. 12.03.2019

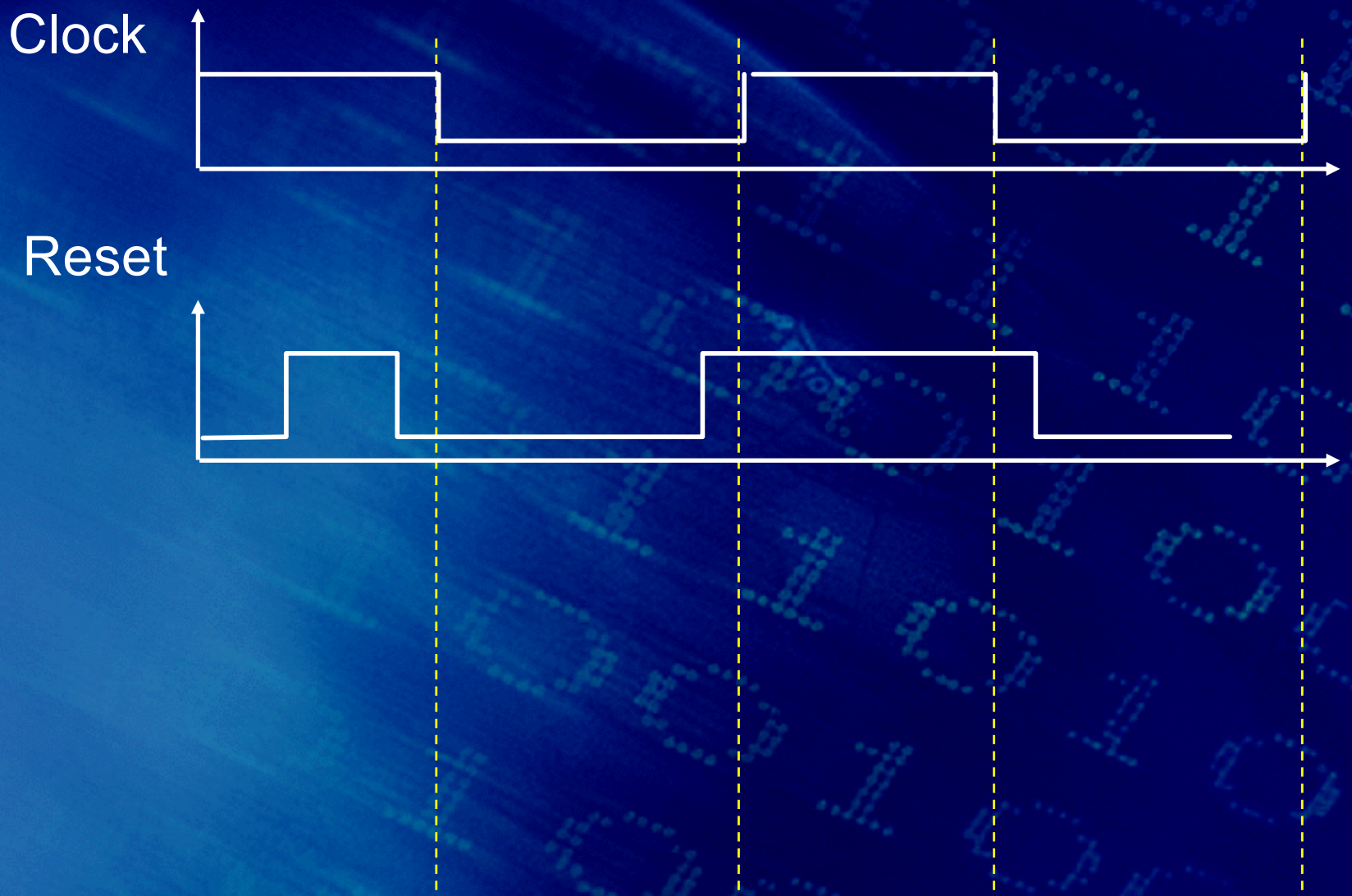
Control Inputs classification

- **According to their asserting characteristics, Control Inputs are usually classified as:**
  - ***Synchronous***
  - ***Asynchronous***

When asserted, they become active at the next clock (edge or pulse), only

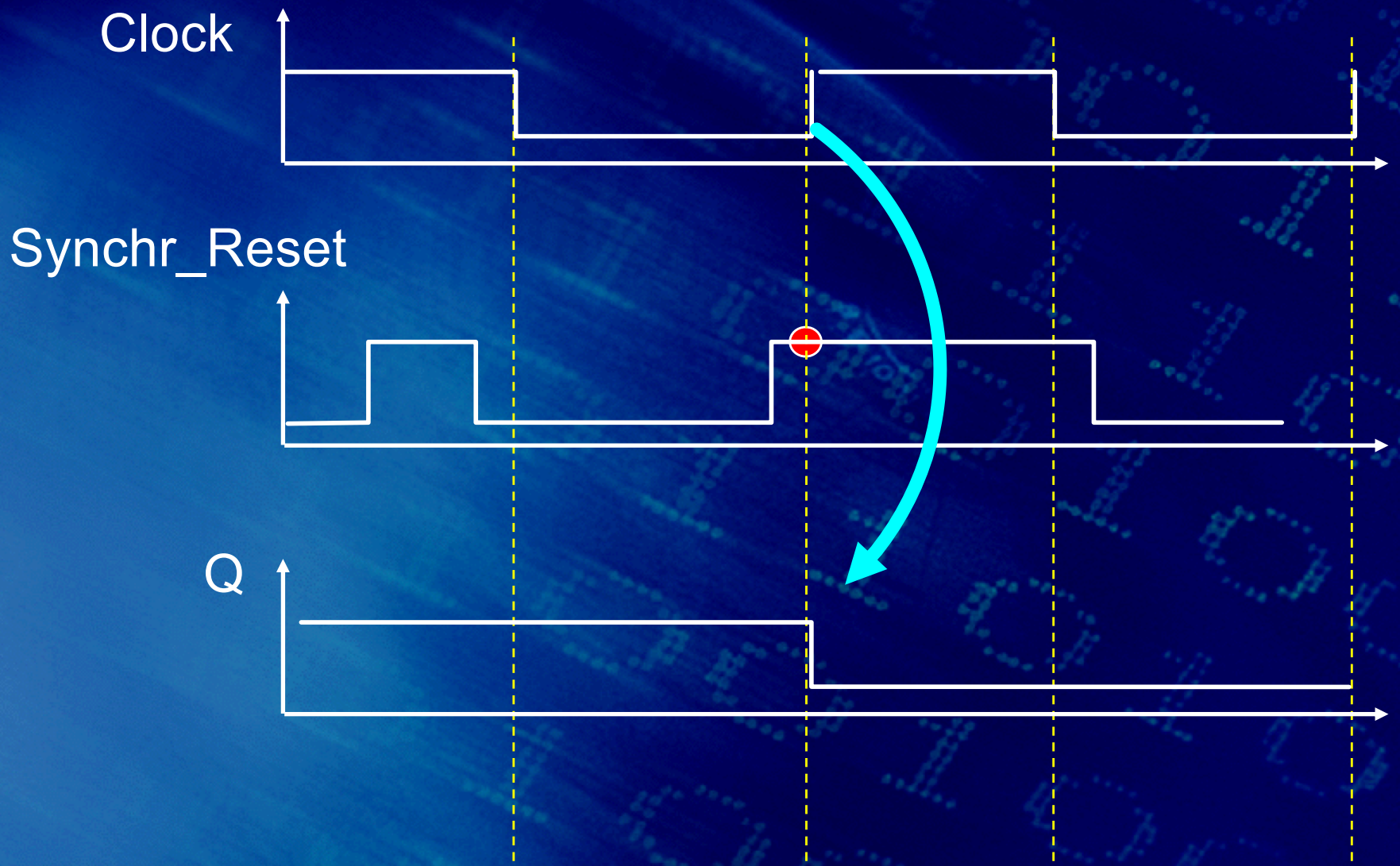
Rel. 12.03.2019

Synchronous reset



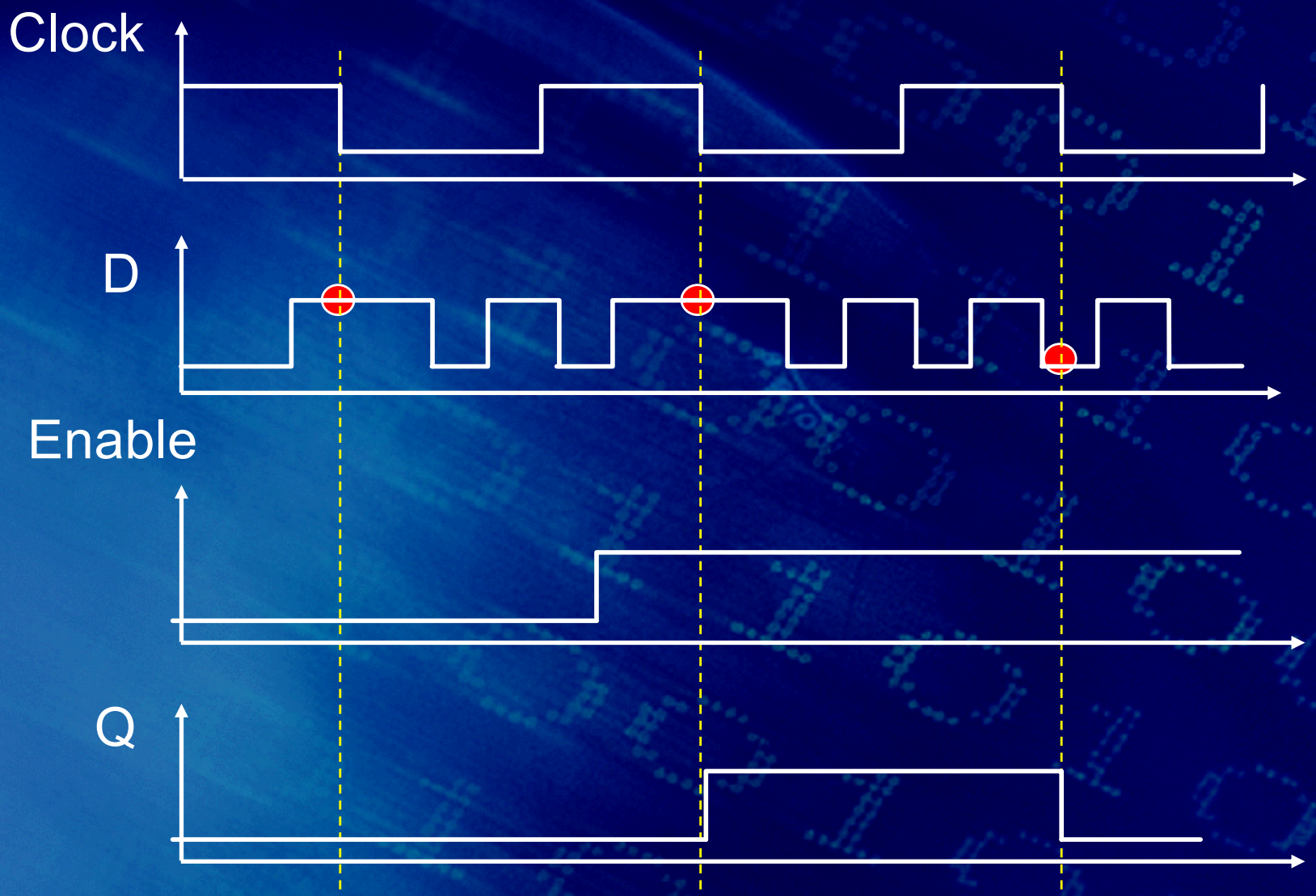
Rel. 12.03.2019

Synchronous reset

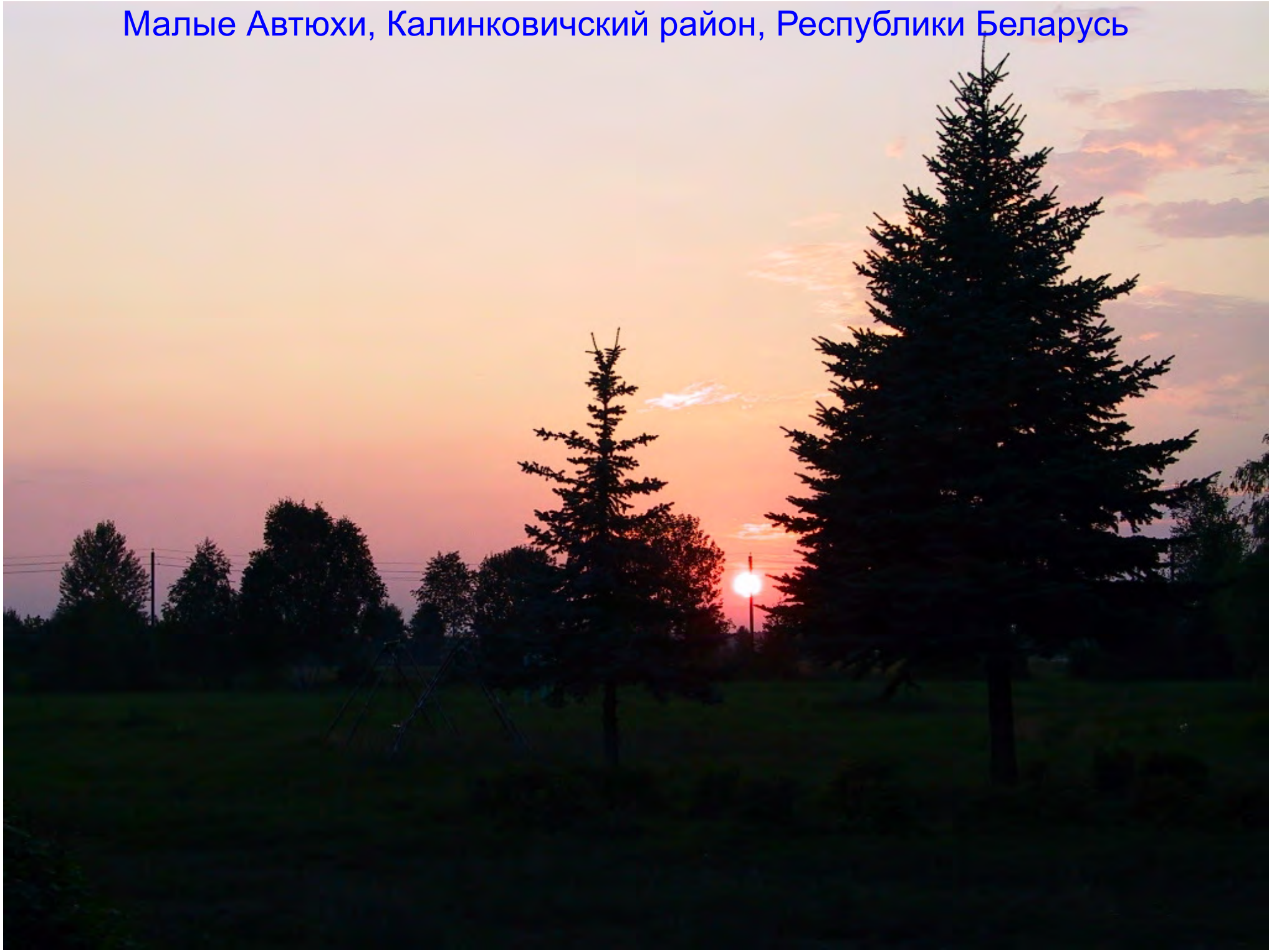


Rel. 12.03.2019

Enable



Rel. 12.03.2019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