Lecture
0_3.1

Semiconductor Technology trends

cini
Cybersecurity
National Lab

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Goal

- This lecture aims at presenting the current trends in the microelectronic industries, with peculiar emphasis on some recent developments, such as SoC, SiP, 3D packaging, and NoC.

Prerequisites

- None

Homework

- Students are warmly invited to visit:
  - web pages related to microelectronic trends
  - web pages of the Intel site related to the Moore's law:
    - www.intel.com/technology/mooreslaw/index.htm
  - web pages on 3D technology advances:
    - www.youtube.com/watch?v=WiTus-tspfA&feature=em-uploademail

Further readings

- The International Technology Roadmap for Semiconductors home page at
  - http://public.itrs.net

Further readings

- **Students interested in making a reference to a text book on the arguments covered in this lecture can refer, for instance, to:**
  - ***G. Conte, A. Mazzeo, N. Mazzocca, P. Prinetto*: "Architettura dei calcolatori", *Città Studi, 2015* (App. C - Evoluzione Tecnologica) (In Italian)**

Outline

- Moore's law
- Advances in *components*:
  - System-on-Chip (SoC)
  - IP-cores
- Advances in *architectures*:
  - MPSoC
- Advances in *packaging*:
  - Advances in Device packaging
  - Advances in System packaging
- Advances in *on-chip communications:*
  - Network-on-Chip (NoC)

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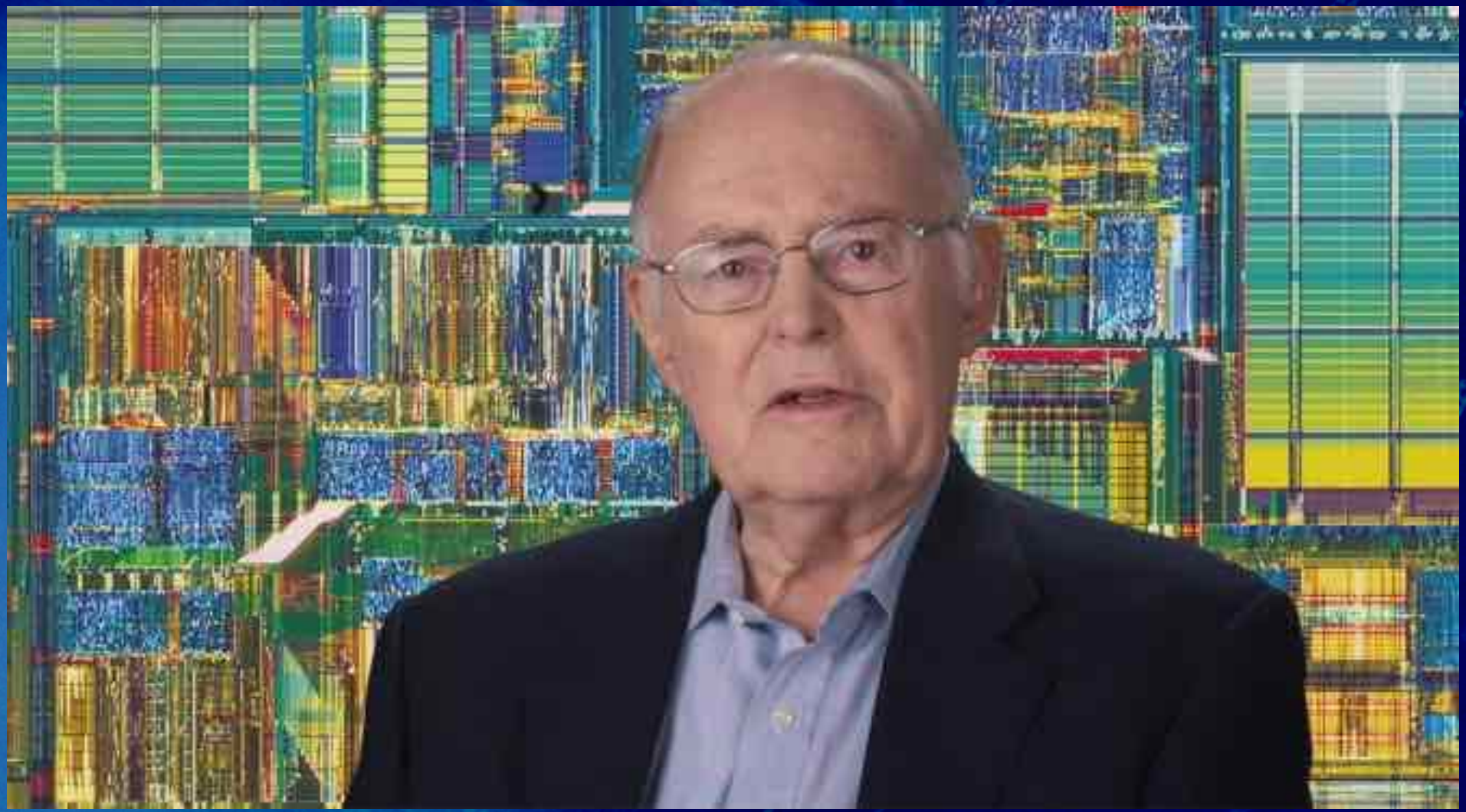
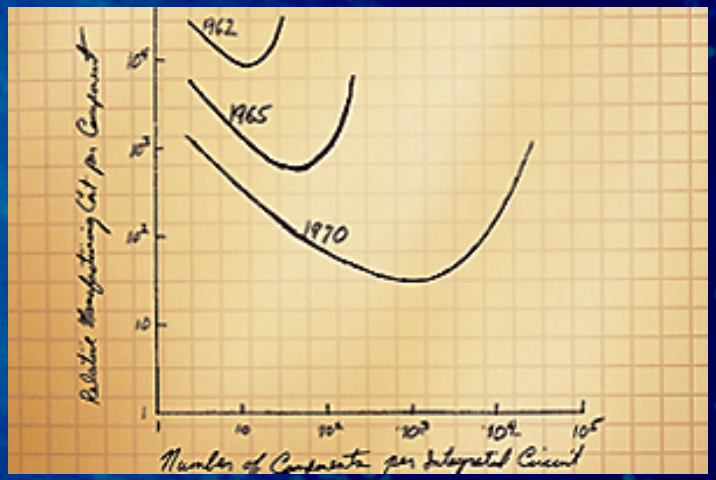
Moore's law



Moore's law

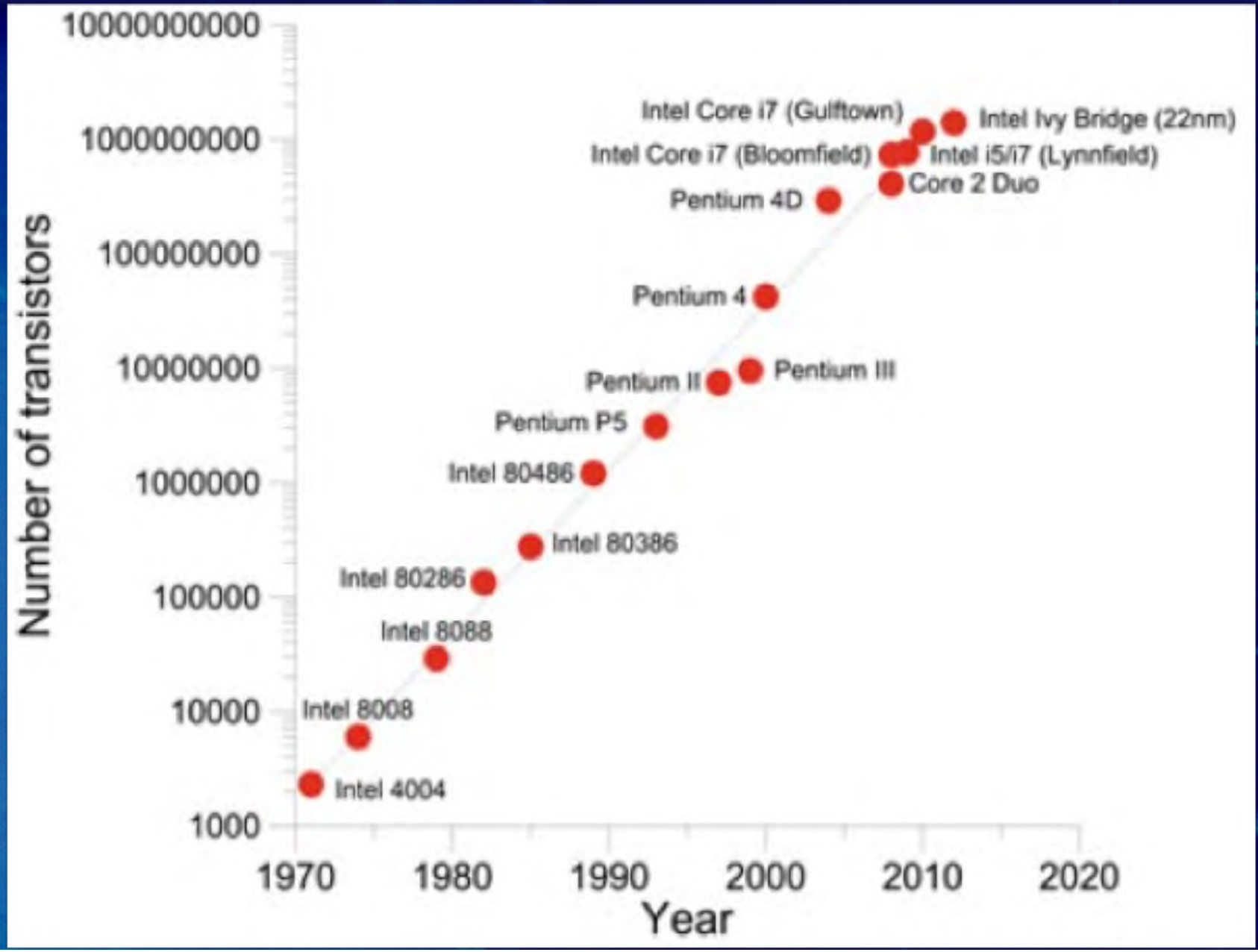
Processor transistor counts doubles every two years



Gordon Moore's original graph from 1965

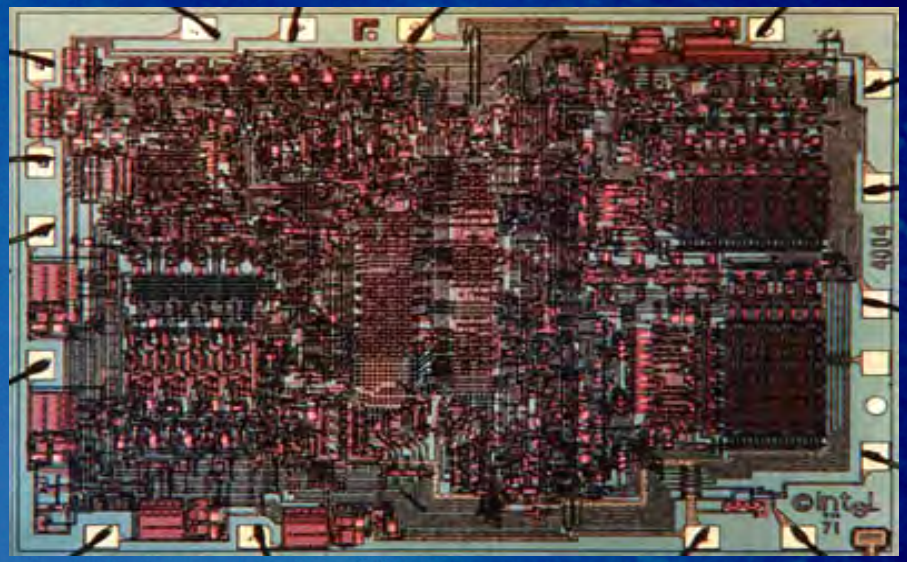
http://www.intel.com/technology/mooreslaw/index.htm

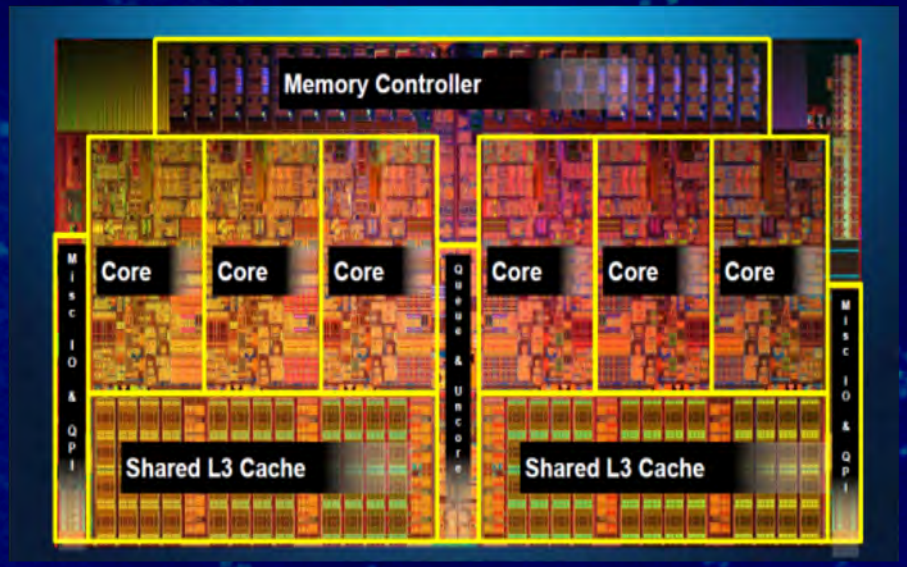
Moore's Law


Number of transistors
10000000000
1000000000
100000000
10000000
1000000
100000
10000
1000
Intel Core i7 (Gulftown)
Intel Ivy Bridge (22nm)
Intel Core i7 (Bloomfield)
Intel i5/i7 (Lynnfield)
Core 2 Duo
Pentium 4D
Pentium 4
Pentium II
Pentium III
Pentium P5
Intel 80486
Intel 80386
Intel 80286
Intel 8088
Intel 8008
Intel 4004
1970
1980
1990
2000
2010
2020
Year

Growth

Intel 4004 (1971)





2.3 k transistors

1.8 G transistors

X 780,000

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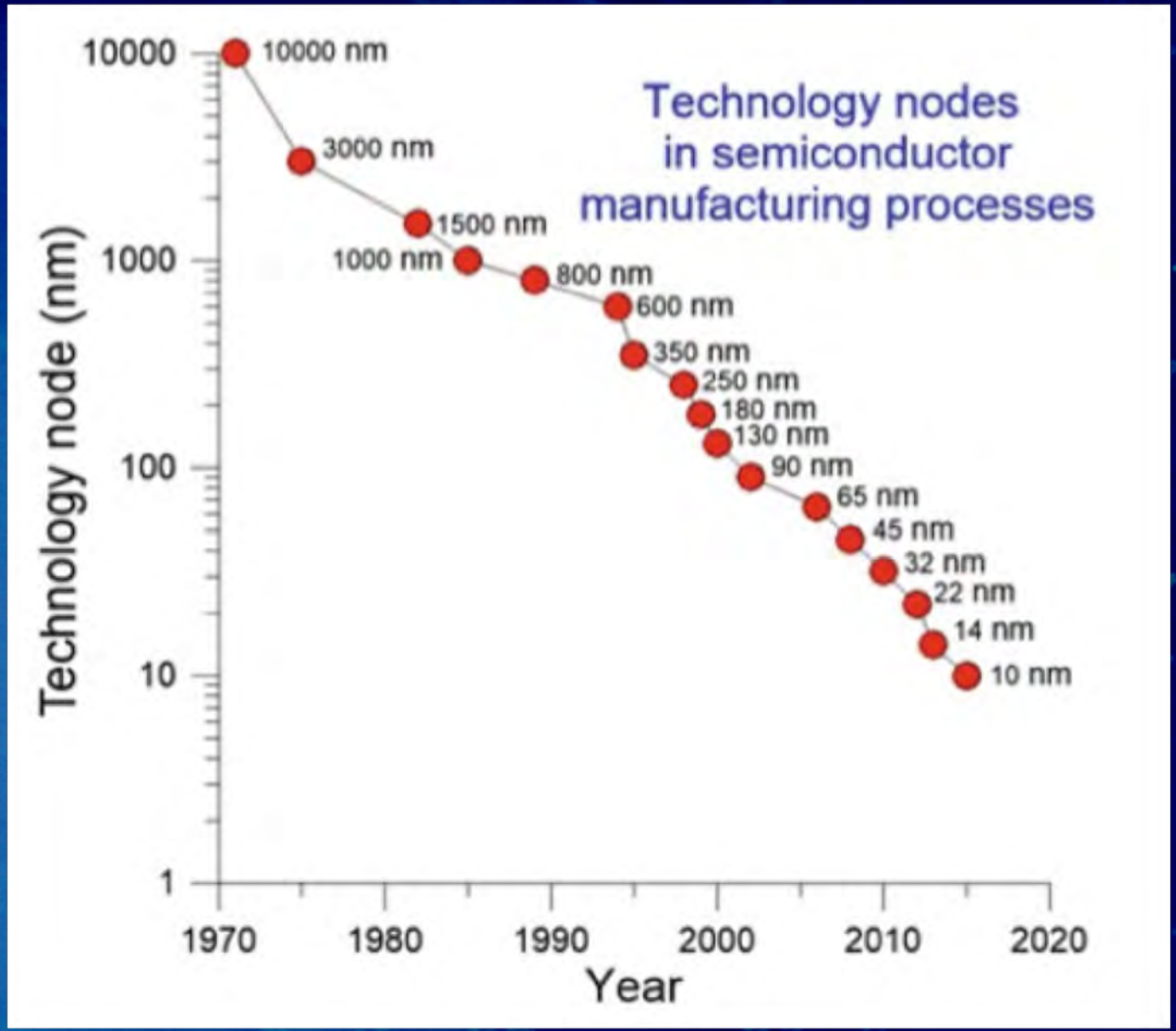
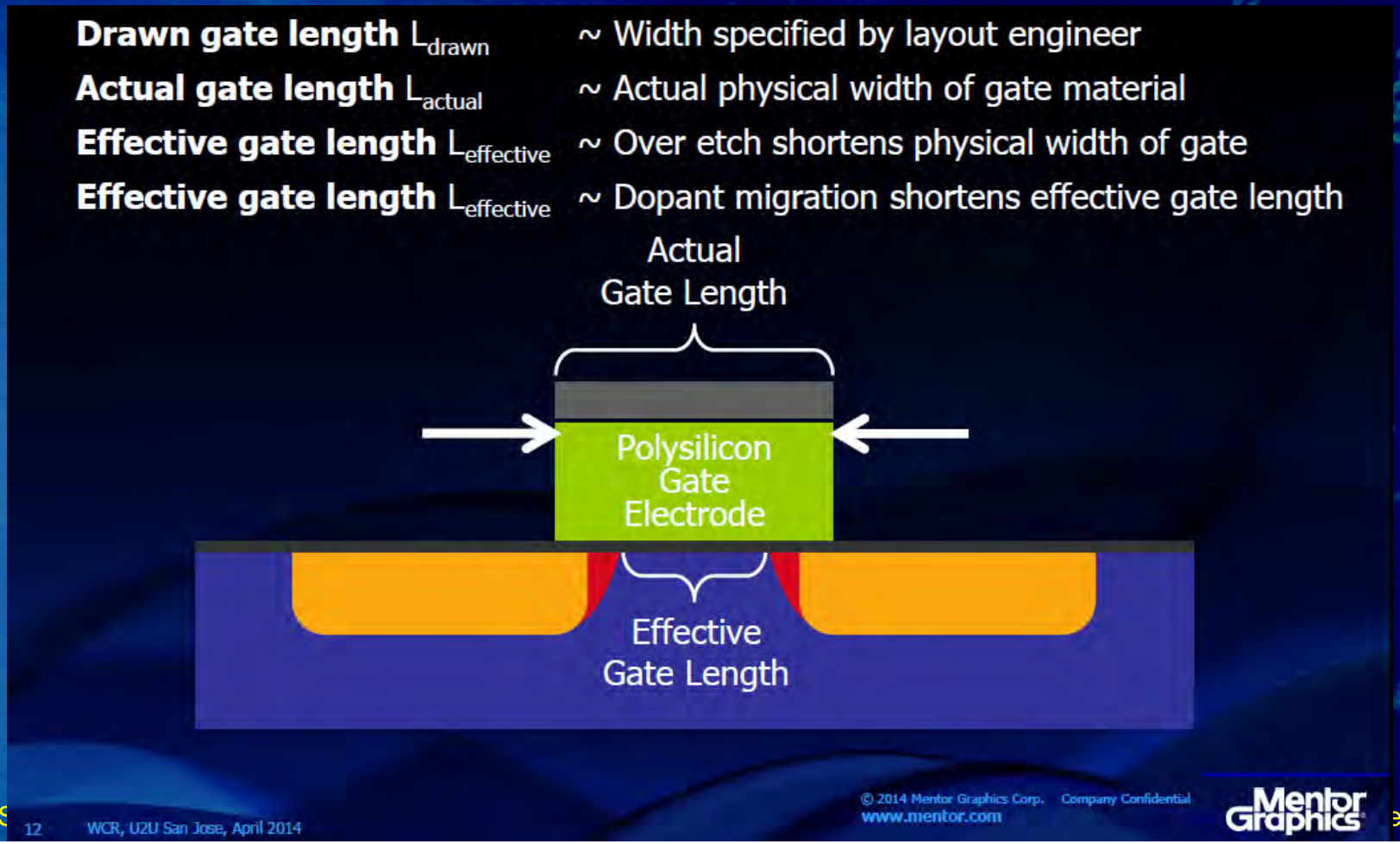
Semiconductor Technology Nodes



Technology node

- **The technology node is traditionally defined as the first layer metal half-pitch or the gate length in the fabrication process**



SoC trends

Yesterday's PCBs

(System-on-a-board)

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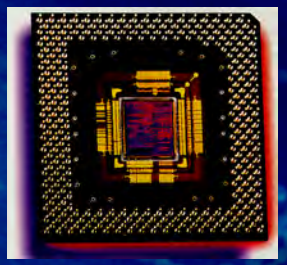
SoC trends



Yesterday's PCBs

(System-on-a-board)

Today's chips
(System-on-a-chip)

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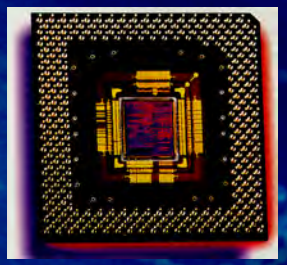
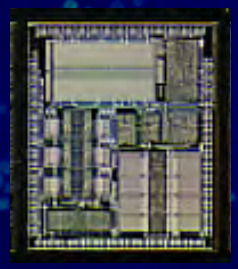
SoC trends

Yesterday's PCBs

(System-on-a-board)



Today's chips
(System-on-a-chip)



Tomorrow's re-usable IP-cores

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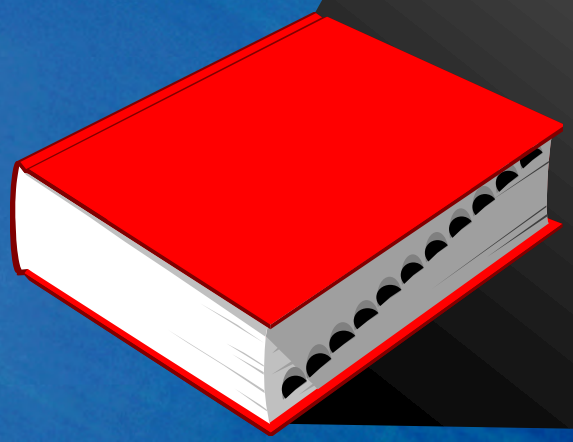
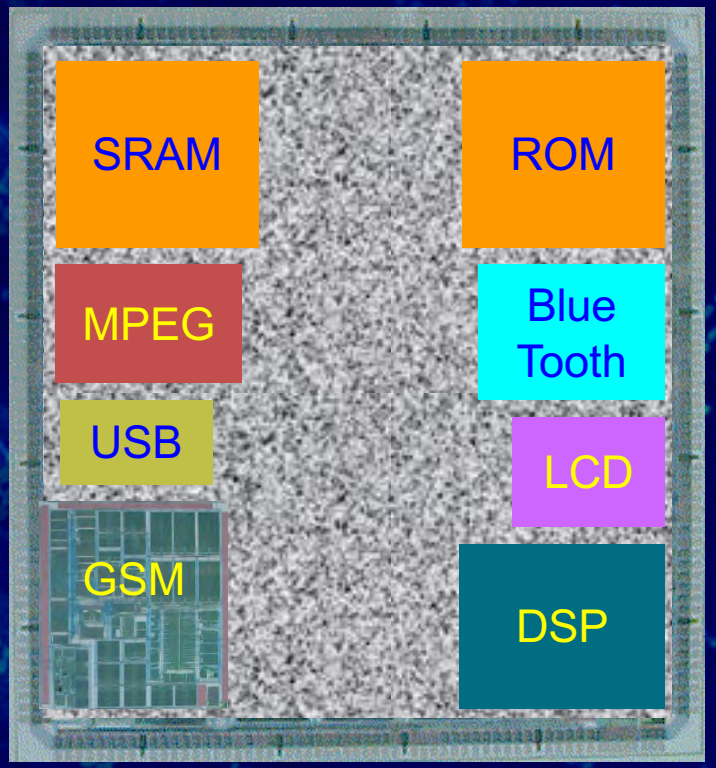


IP core

A hardware circuit design implementing a well-defined set of functions that is lent, sold, or licensed from one provider to a customer

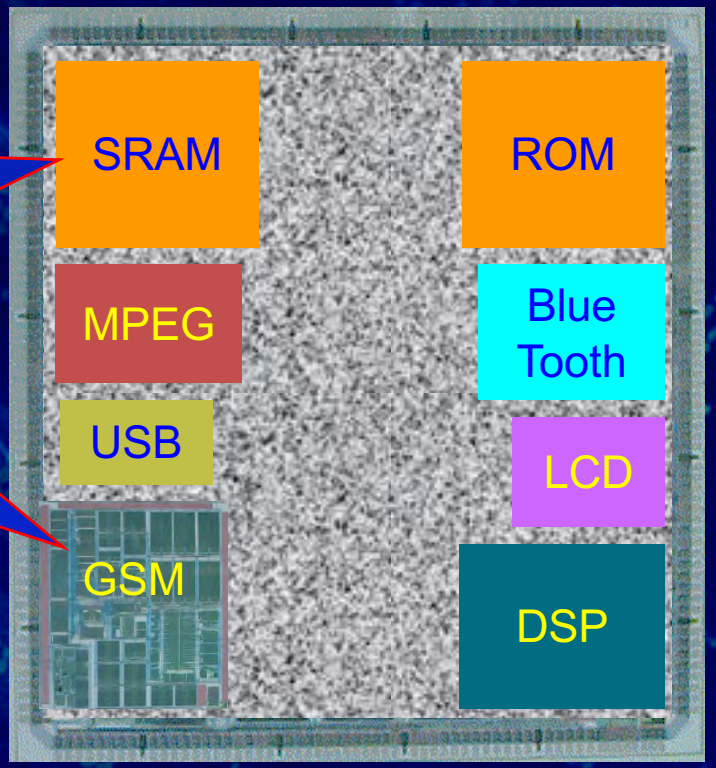
An example

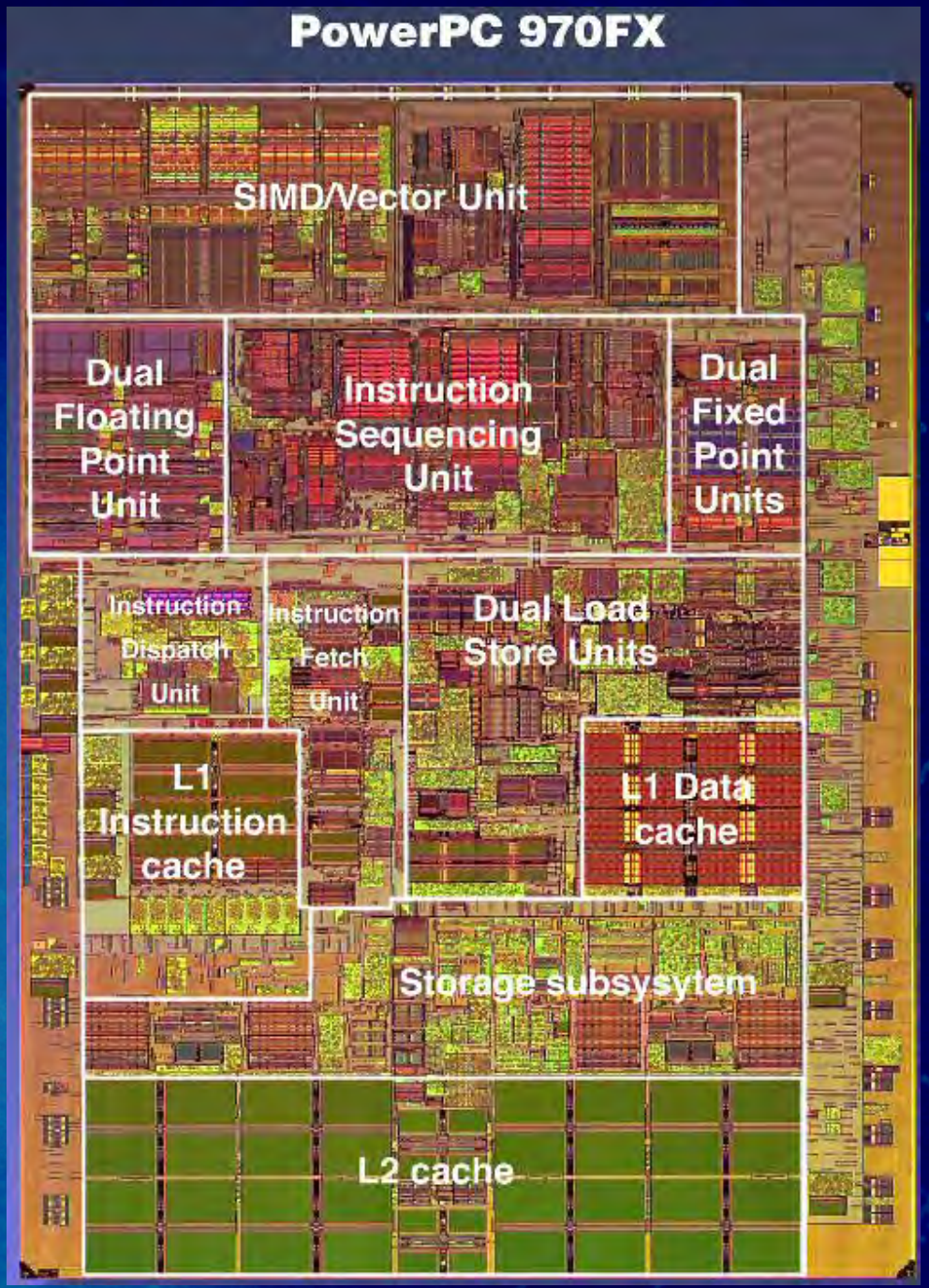


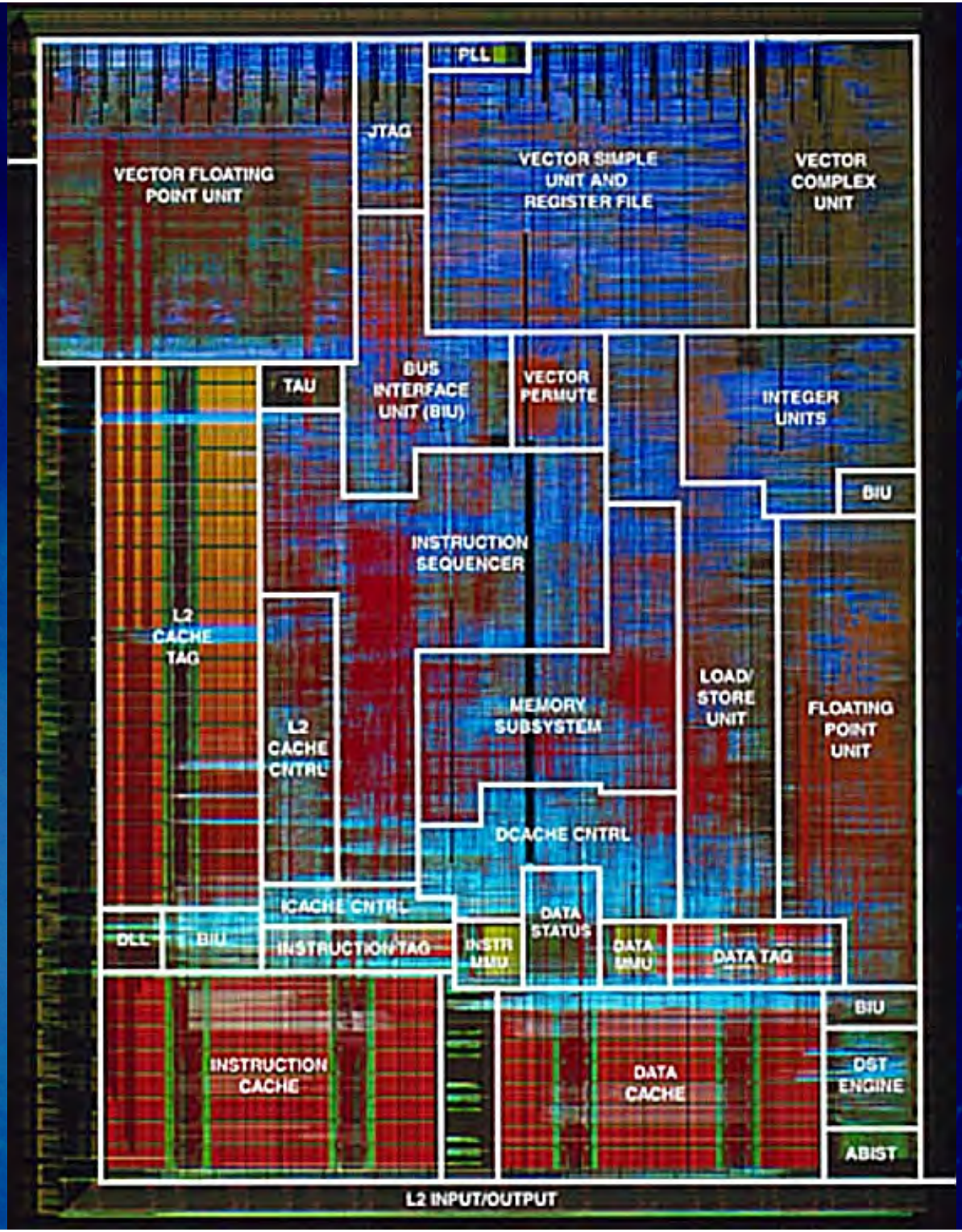
An example

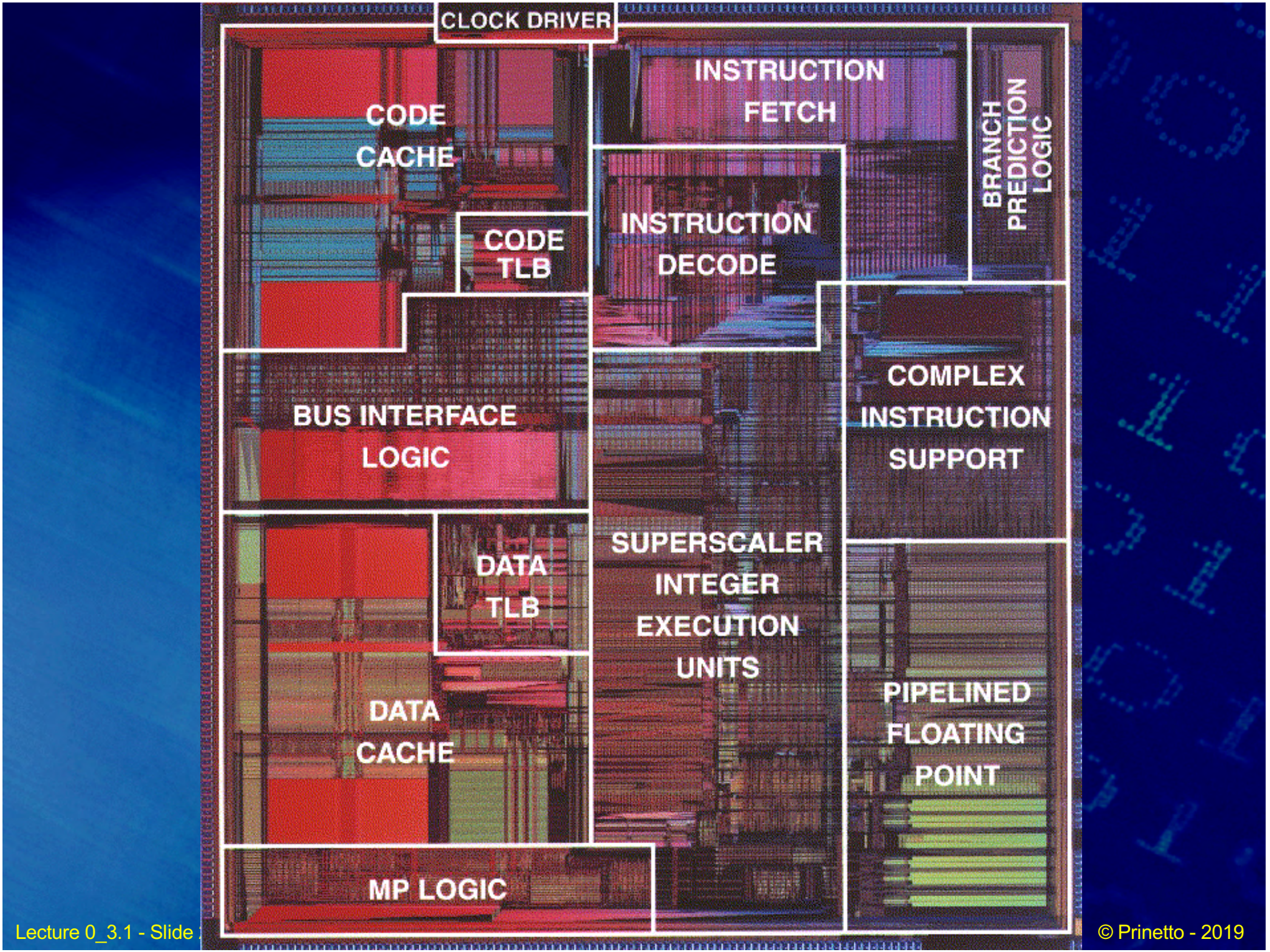
Embedded Cores:

Pre-designed, pre-verified functional blocks, also termed *IP* (Intellectual Property), or *macro*.









Costs

High costs for design

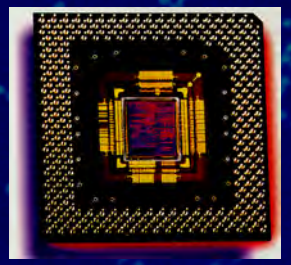
- **The design cost for SoC at 28 nm counted up to**

  80 - 100 M US $

  due to increasing NRE costs
- **Total SoC design costs increased 89% from the 28nm node to the 14nm node and are expected to increase 32% again at the 10nm node and 45% at the 7nm node.**
- **Total Software design costs increased 74% at the 28nm node and are forecast to show a CAGR of 69% through the 7nm node**
- **14nm silicon with a $20.00 ASP is required to ship 9.954M units to reach the breakeven point.**

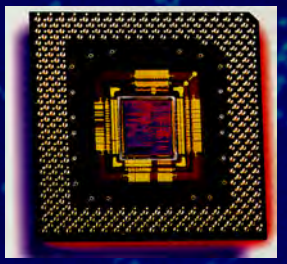
High costs for production

14 nm production line



High costs for production

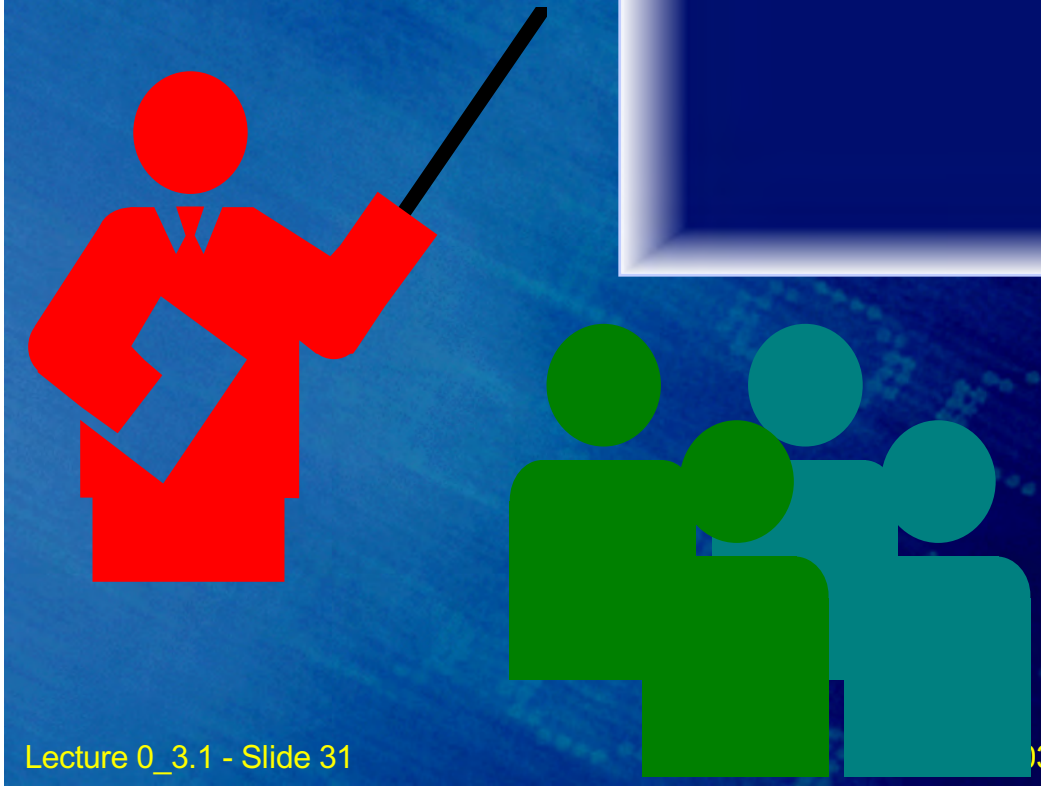
14 nm production line



10+ Billions !!!

Risks

36% of fabs
&
45% of production capacity
are in high risk areas



Risks

Just 4 silicon companies:

- *Samsung*
- *Intel*
- *TMSC (Taiwan)*
- *Global Foundries (UAE)*

Outline

- Moore's law
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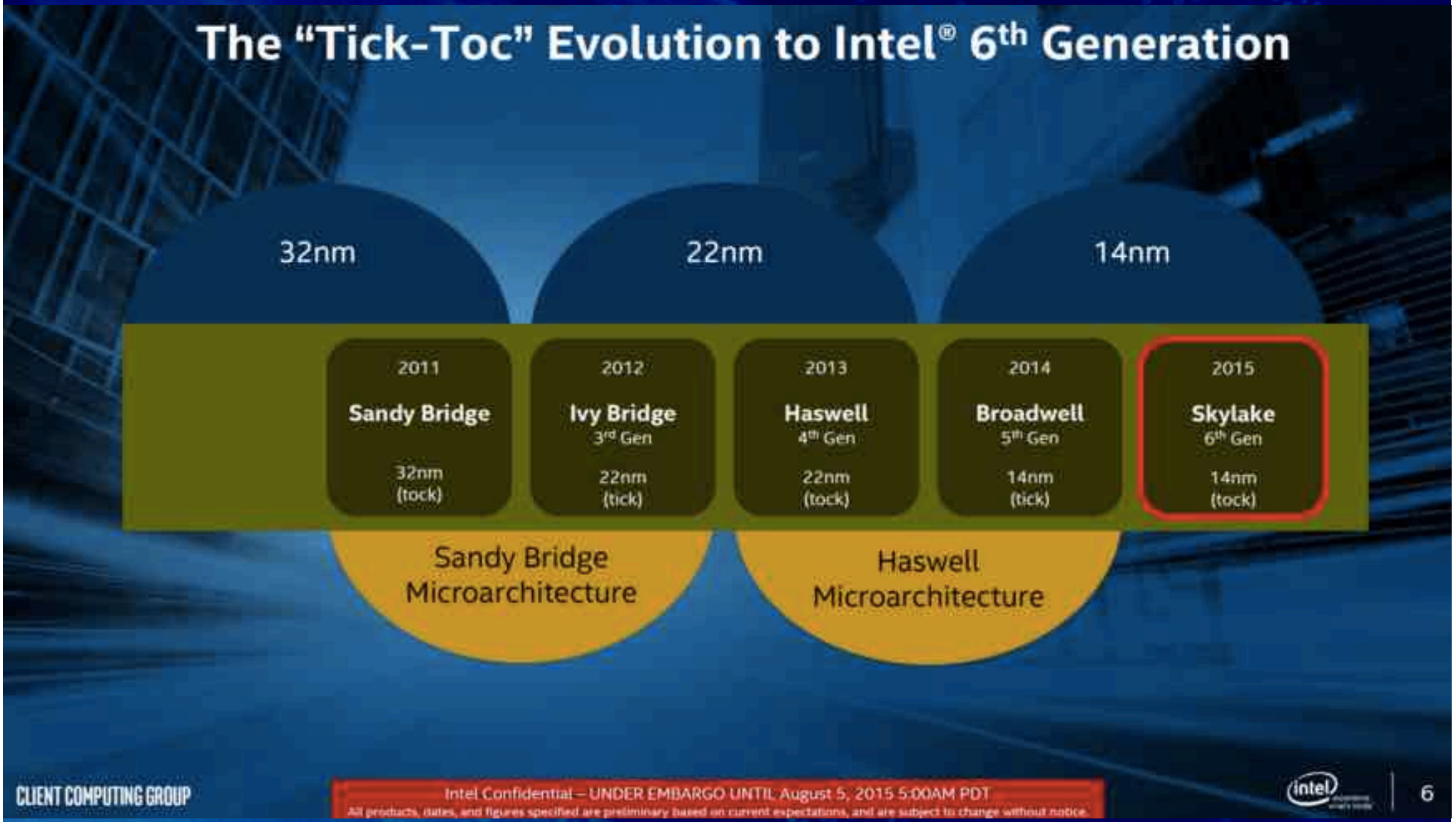
Intel's Tick-Tock Model of chip making



Pollack's Rule

- In a given process technology, performance increase is roughly proportional to square root of increase in complexity

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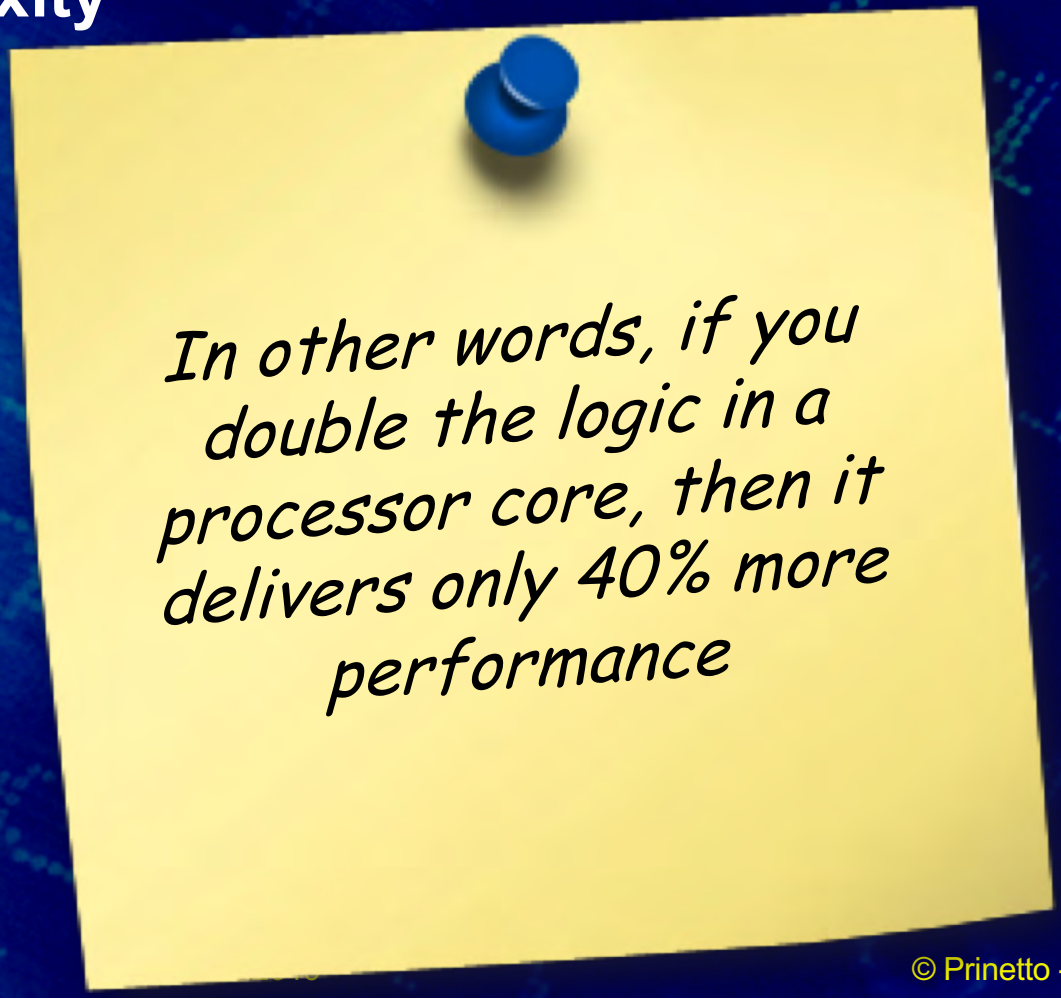

Consequences: MPSoC MultiProcessor SoC Architecture

- They provide near linear performance improvement with complexity and power

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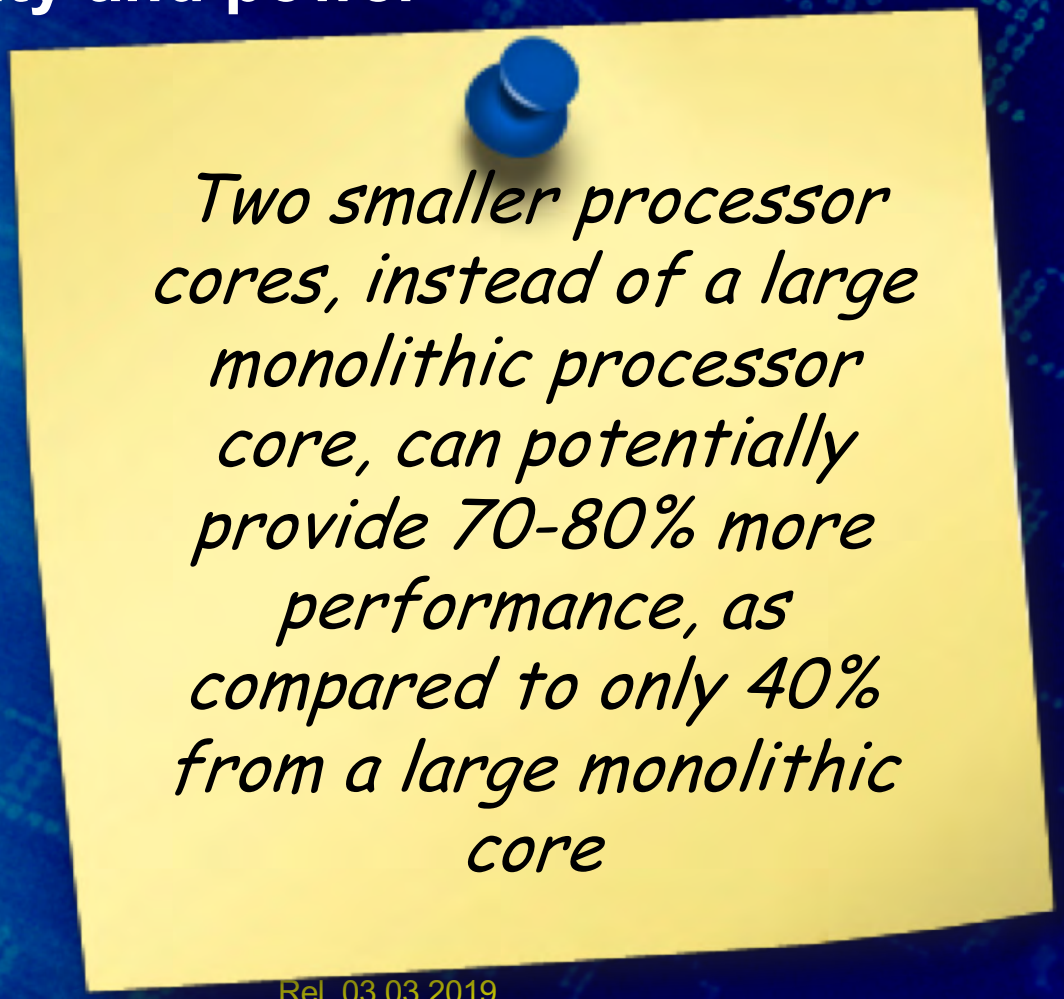
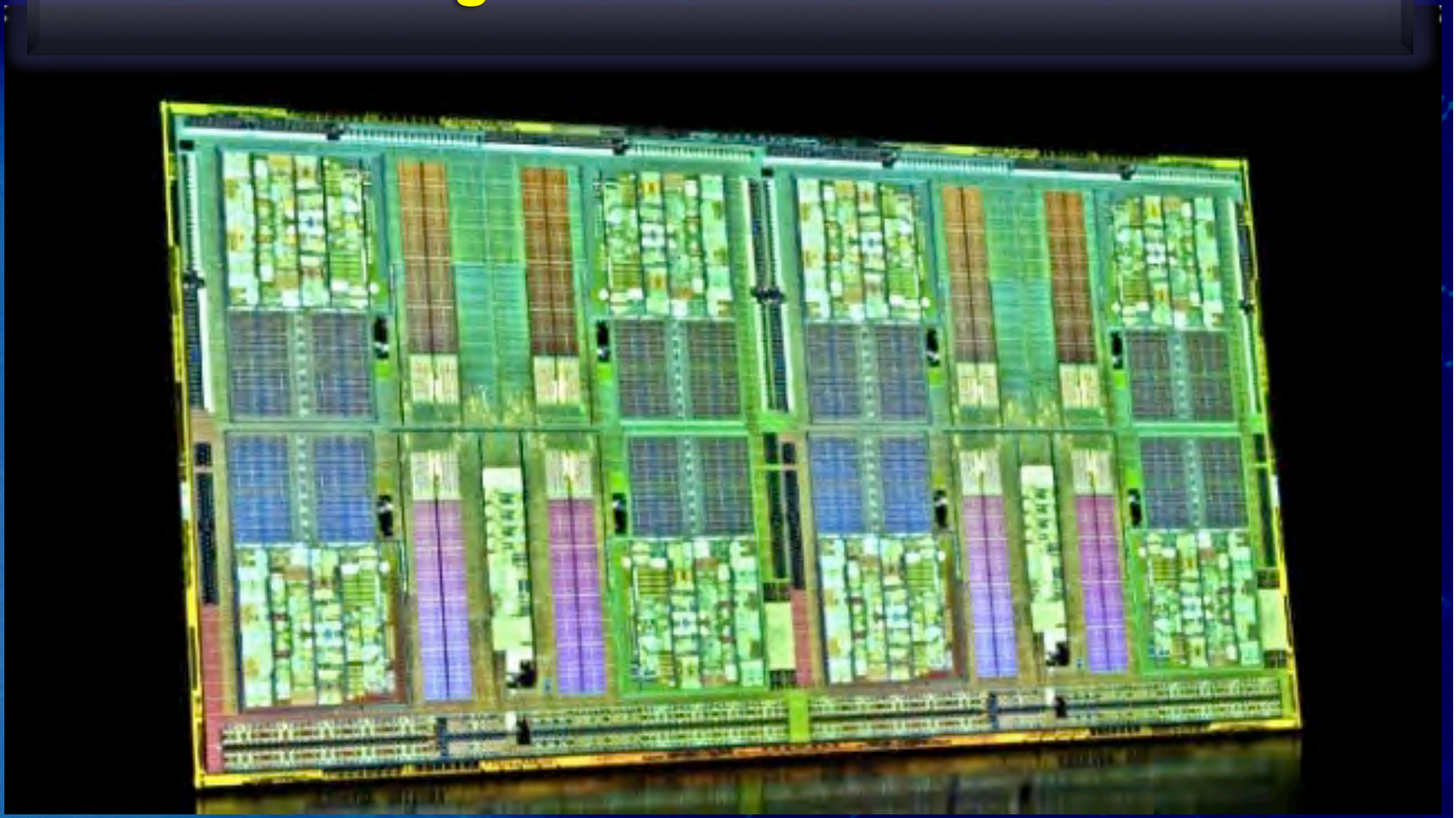


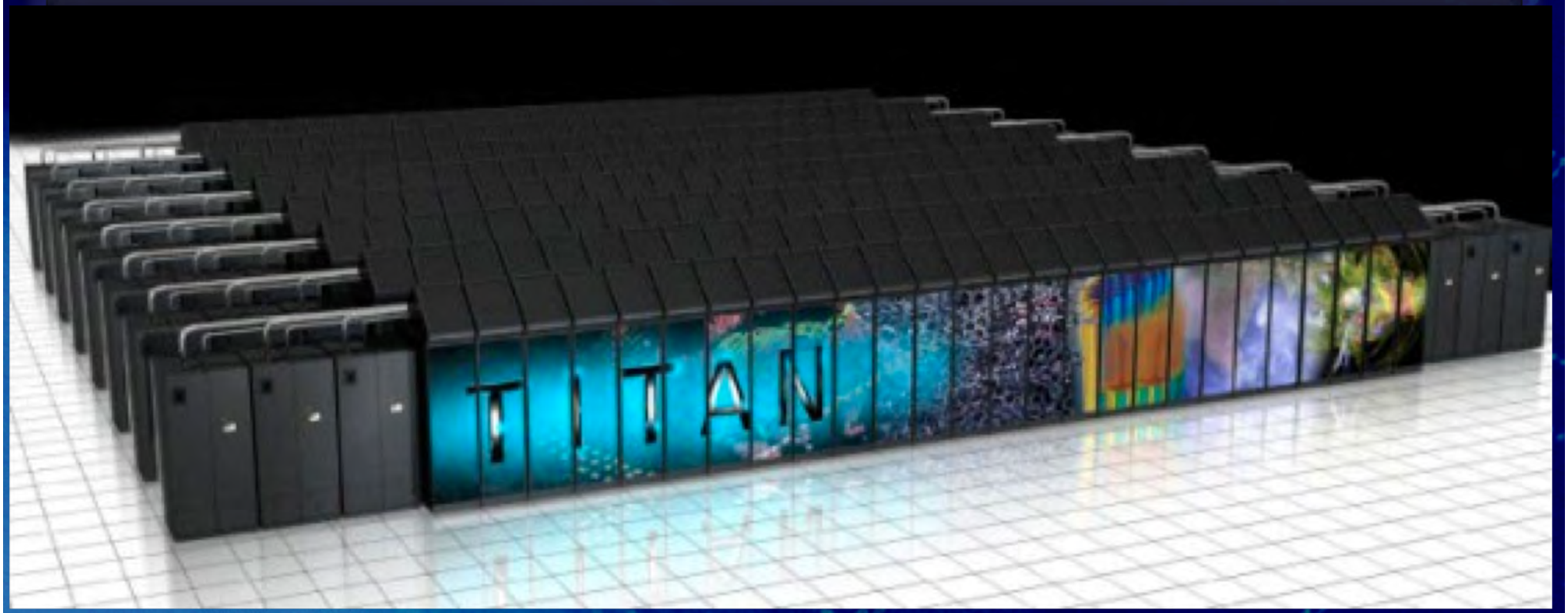
Applying Pollack's rule inversely…

- **Performance of a smaller core reduces as square-root of the size, but power reduction is linear, resulting in smaller performance degradation with much larger power reduction**
- **Overall, the compute throughput of the system increases linearly with the larger number of small cores.**

CPU AMD Opteron including 16 cores x86 at 2.6 GHz



Titan Cray XK7



- 17.59 PFlop/s (10^{15} Flop/s)
- 18,688 CPU AMD Opteron + 18,688 CGPU Nvidia Tesla, for a total of 560,640 processor core
- Consumes 8.2 MW
- Total memory of 700 TB

Multiprocessors additional benefits

- Each processor core can be individually turned on or off, thereby saving power
- Each processor core can be run at its own optimized supply voltage and frequency
- Easier to load balance among processor cores to distribute heat across the die
- Can potentially produce lower die temperatures improving reliability and leakage
- …

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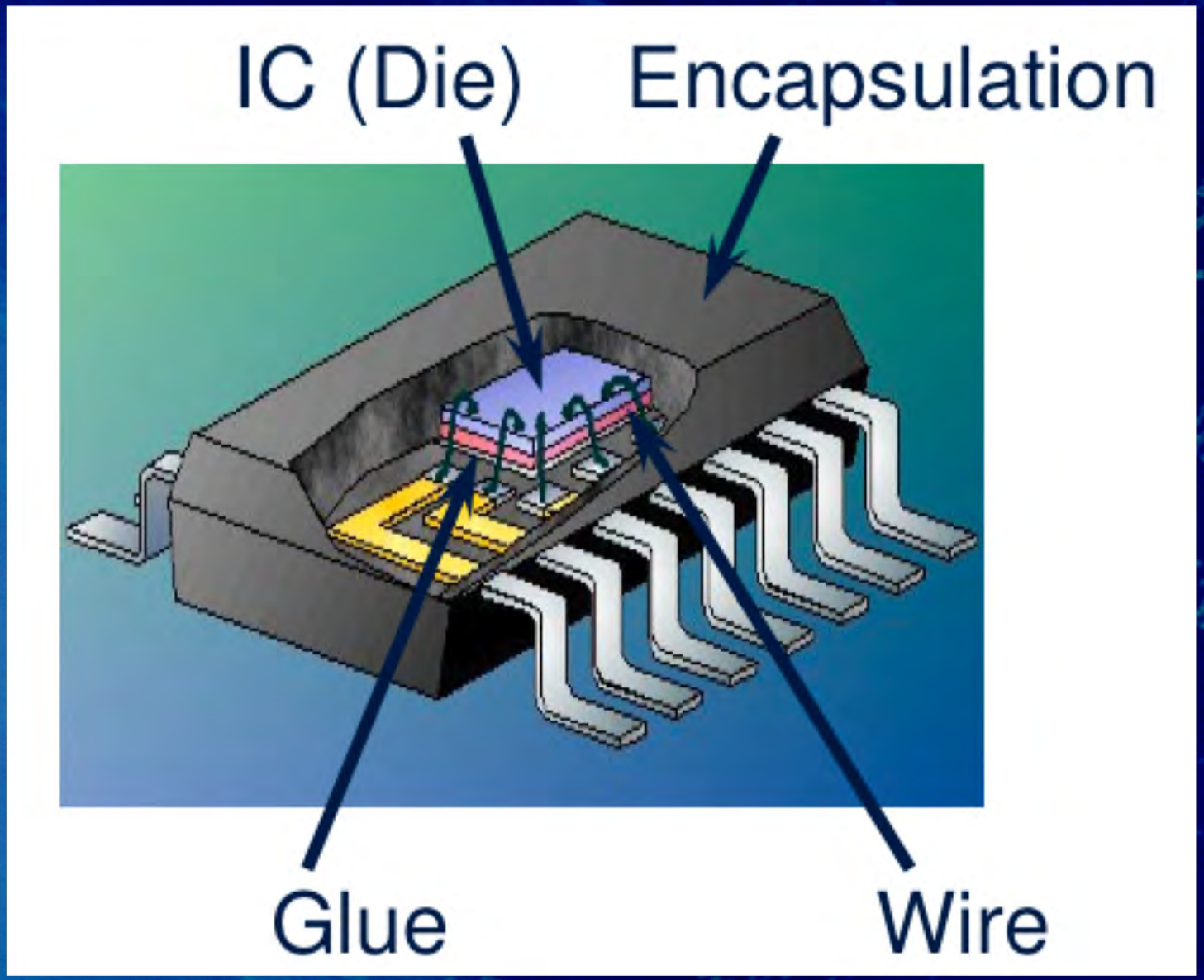
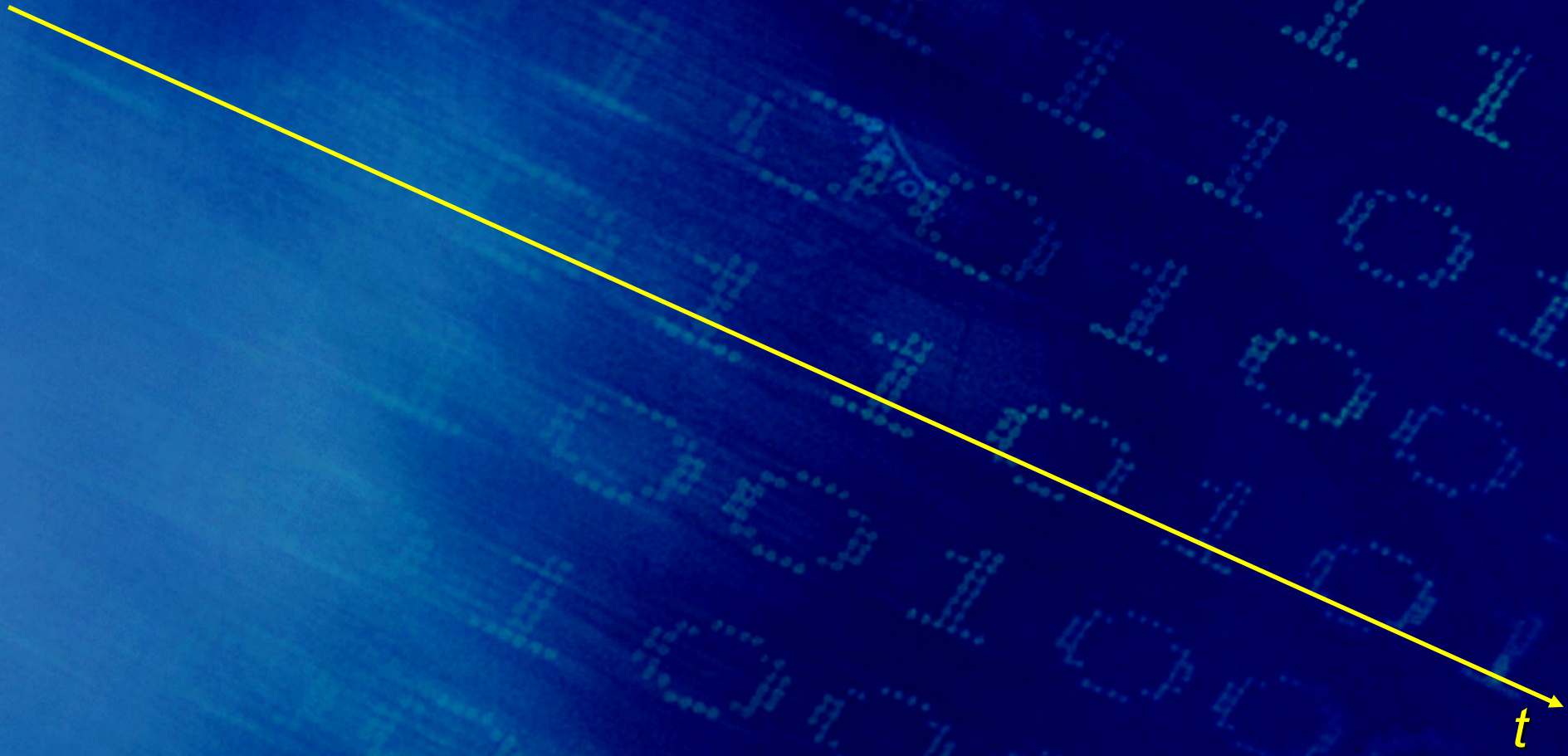
IC's traditional package



Advances in Device Packaging



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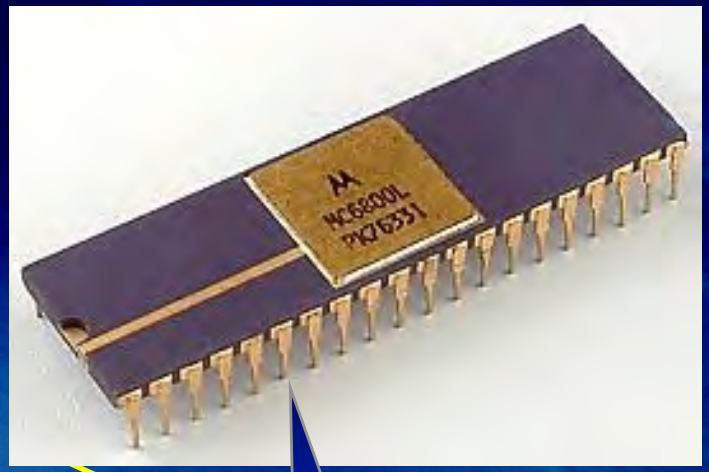

PTH (Pin Through Hole) device

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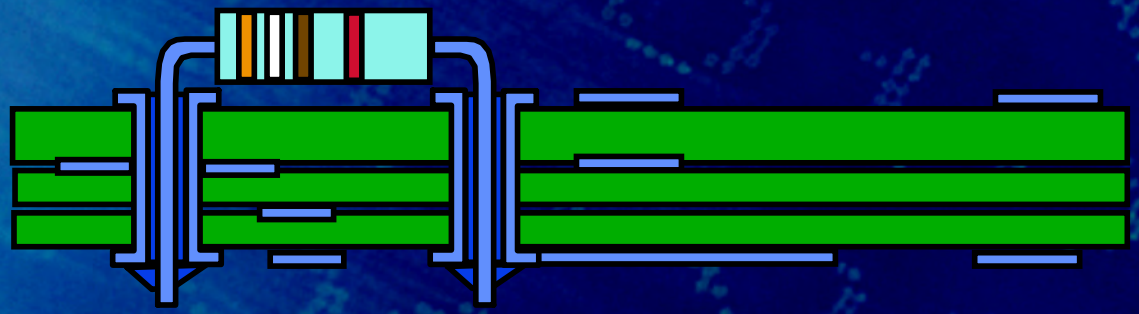
PTH components

PTH (Pin Through Hole) component



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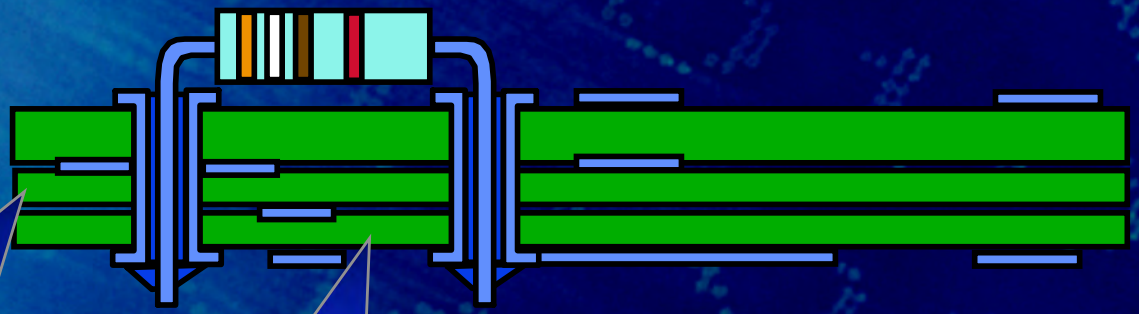
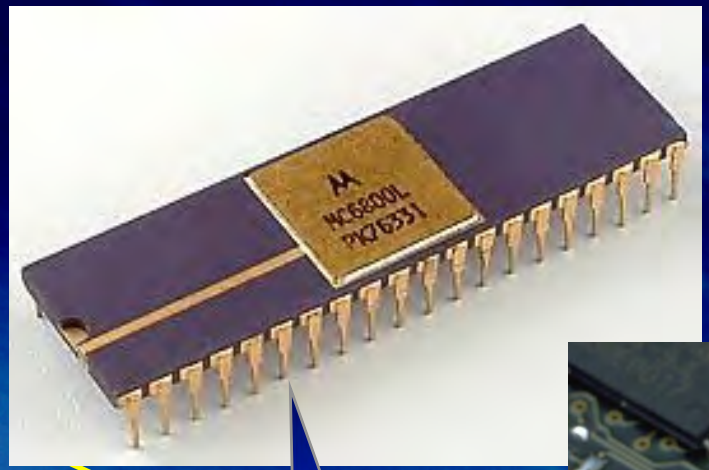
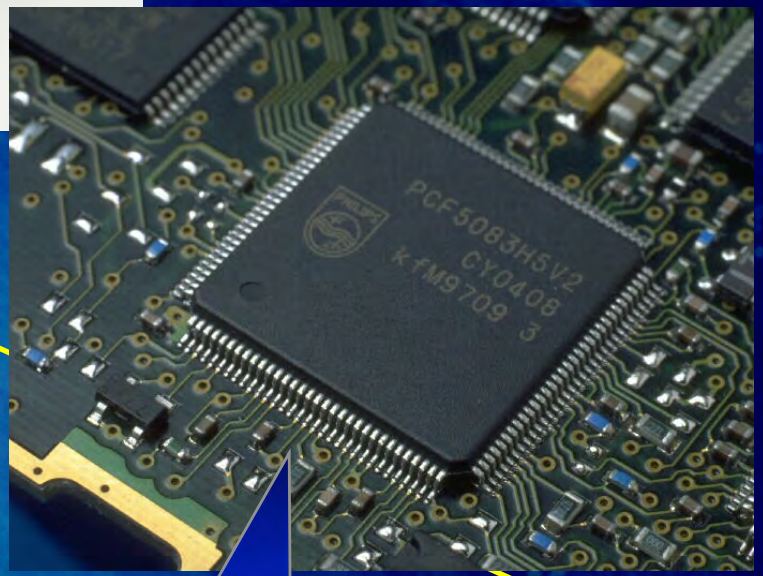


Multi-layer PCB

Up to 12 layers

Advances in Device Packaging





PTH (Pin Through Hole) device

SMD (Surface Mounted Device)

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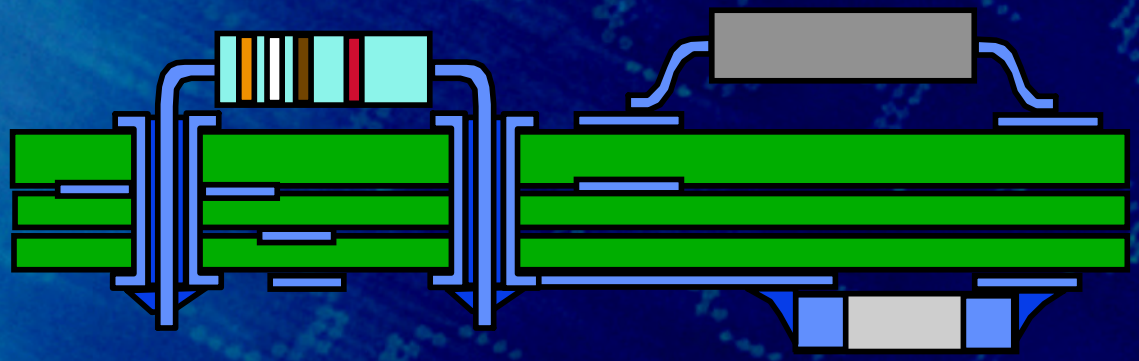
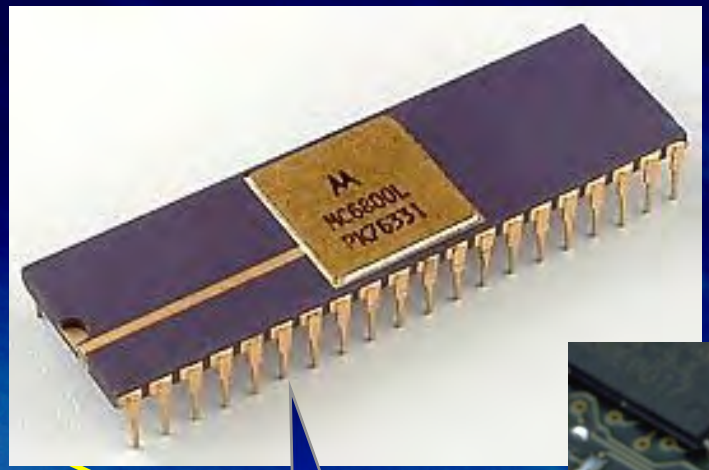
Surface Mount Device

SMD (Surface Mounted Device) component



Advances in Device Packaging



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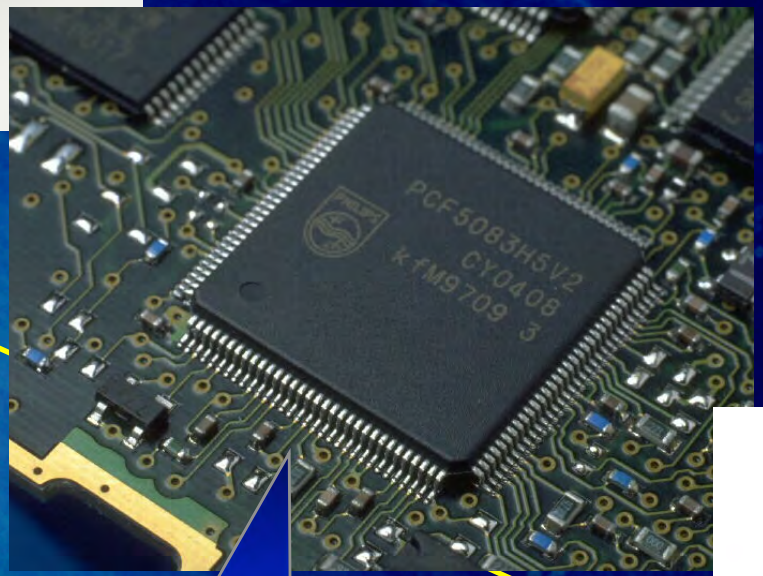
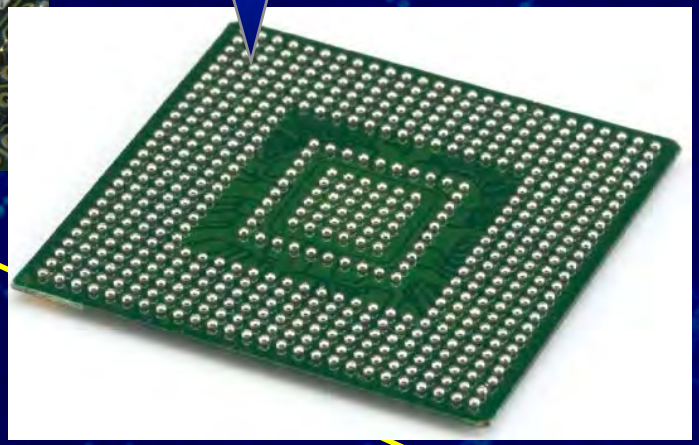


SMD (Surface Mounted Device)

BGA (Ball Grid Array) device



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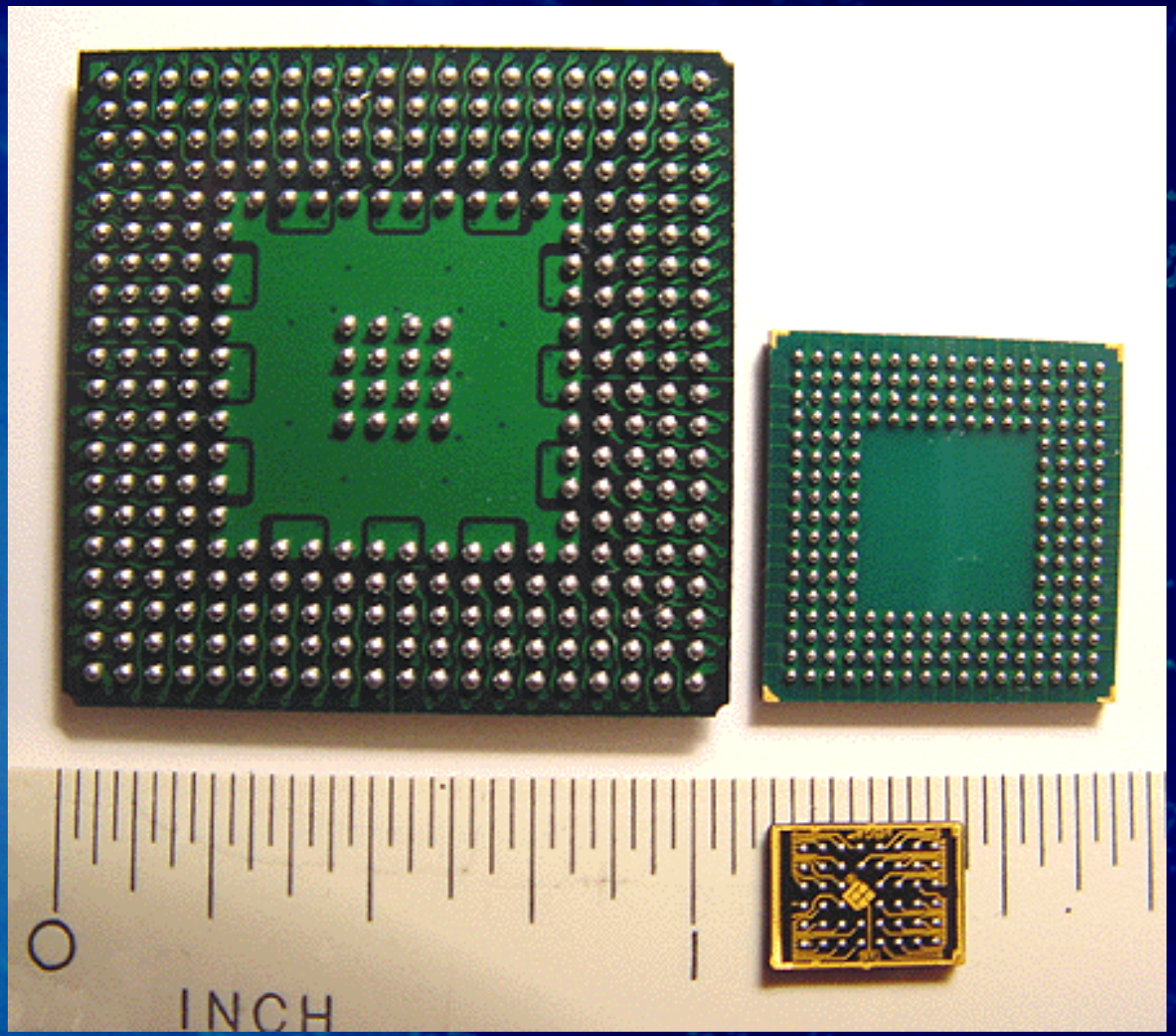
Ball Grid Array



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Advances in System Packaging

PCB (Printed Circuit Board)

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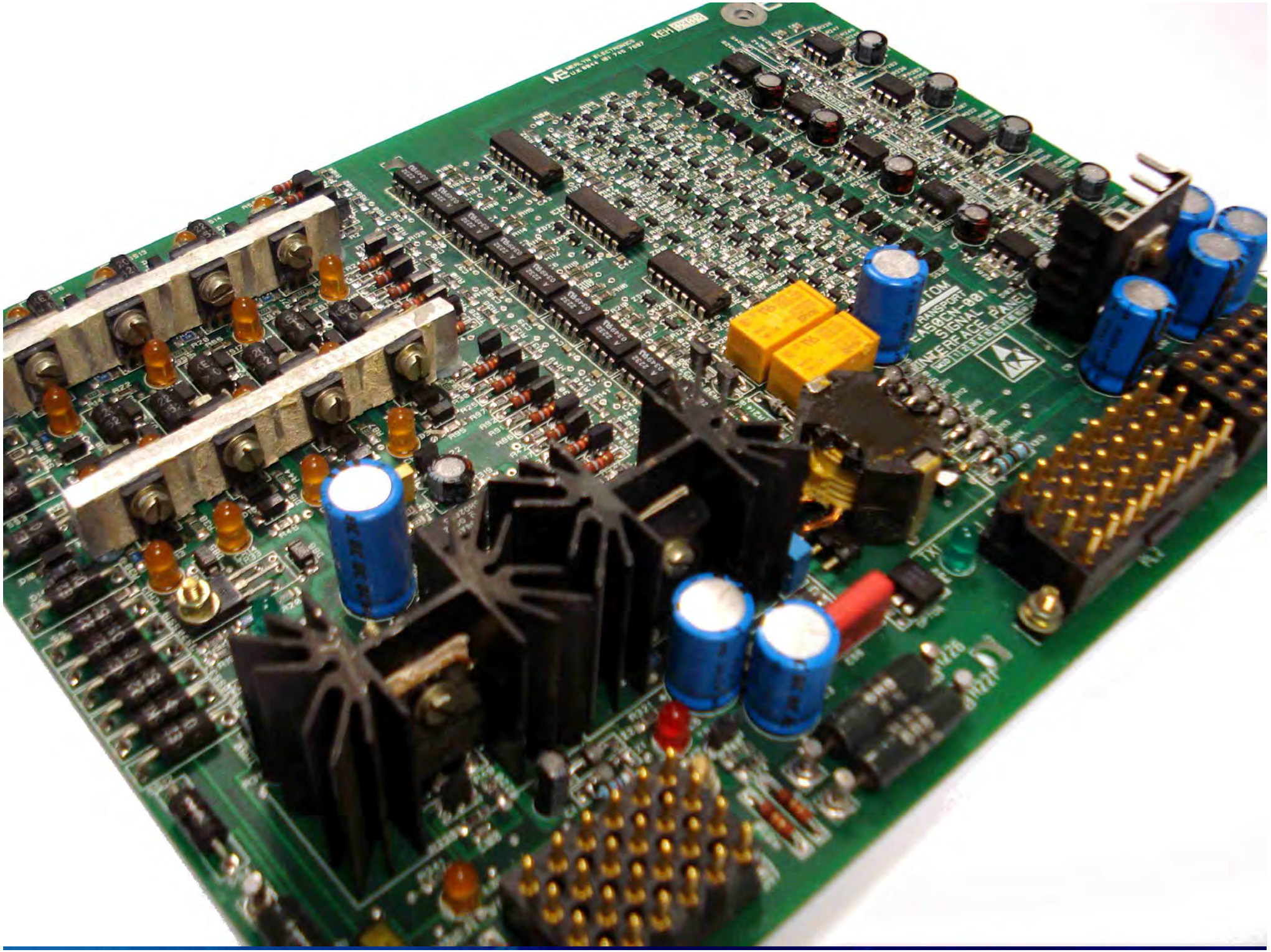
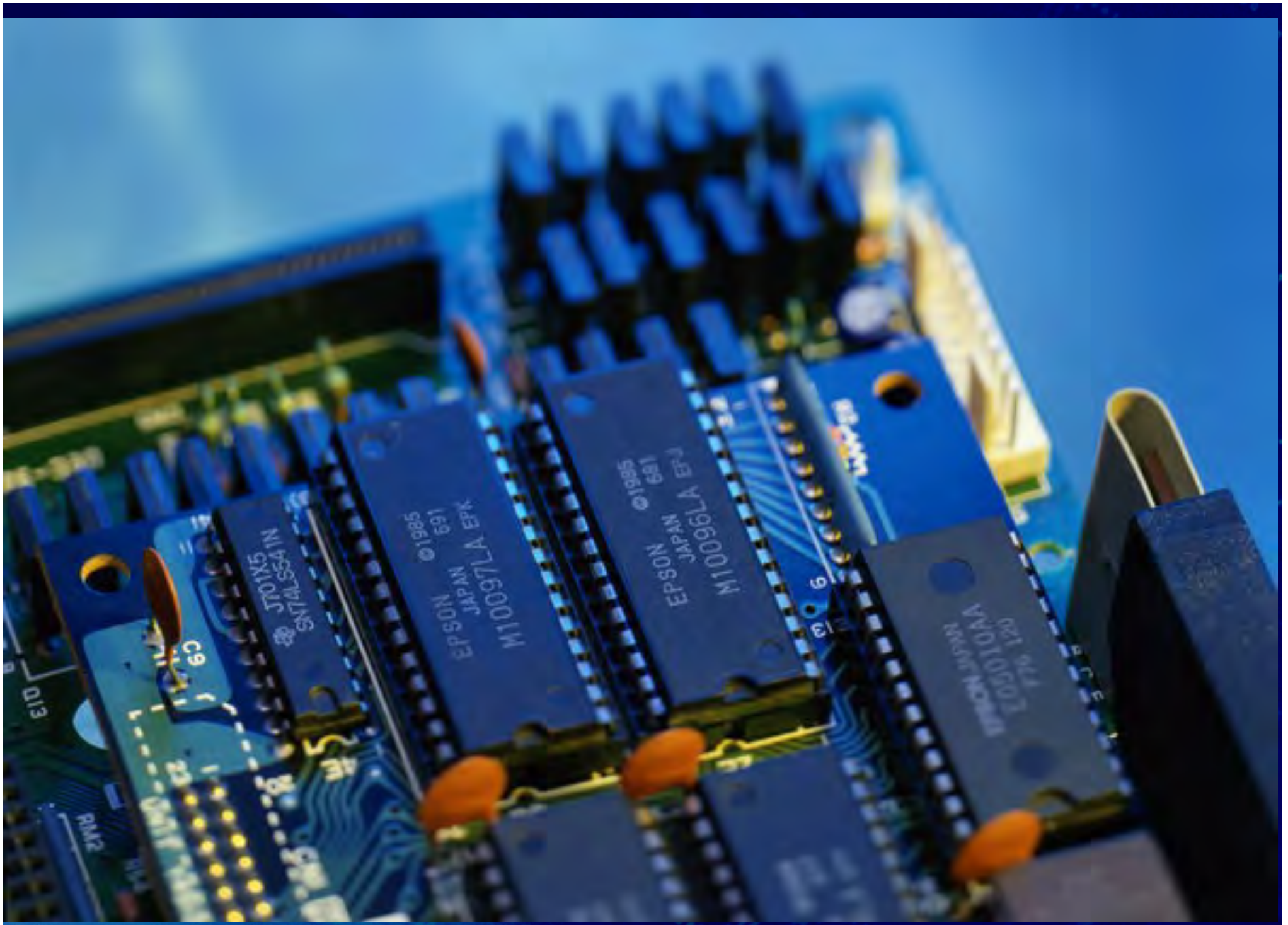
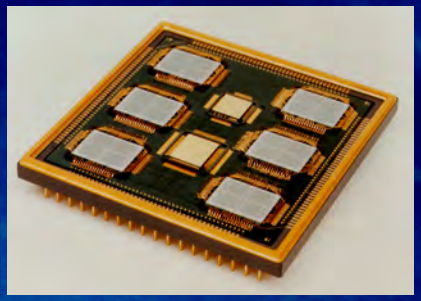

TRANSPORT
SIGNAL
INTERFACE PANEL



Advances in System Packaging



PCB (Printed Circuit Board)

MCM (Multi-Chip Modules)

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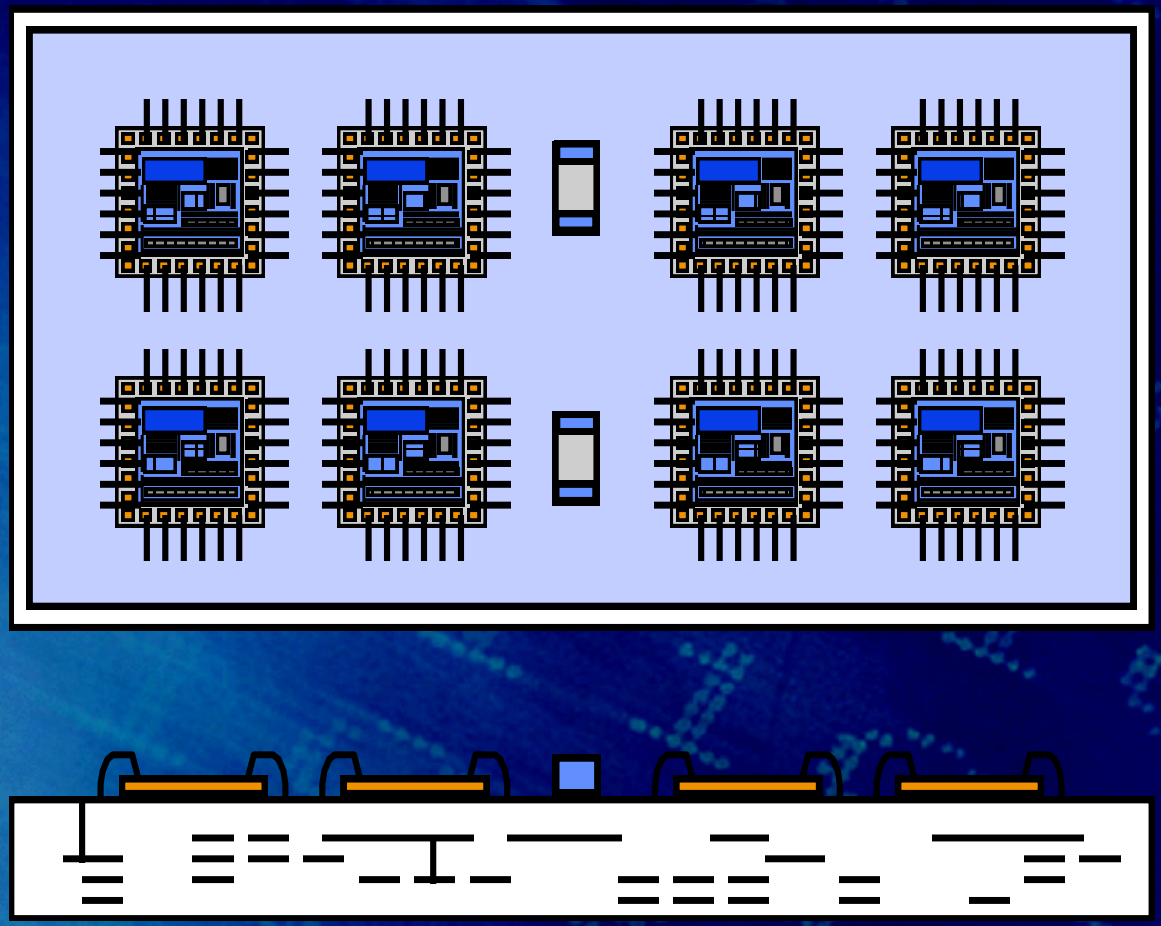
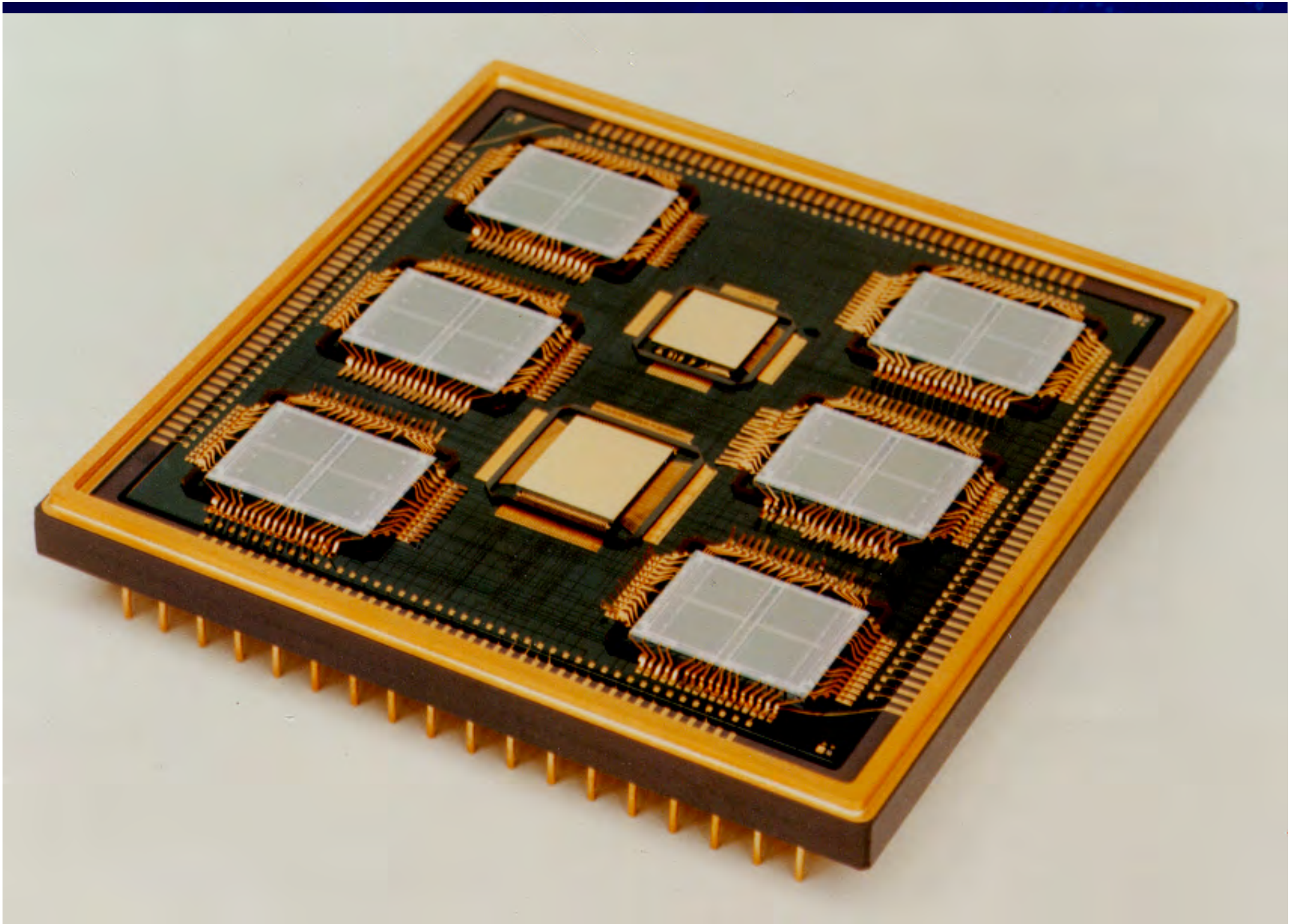
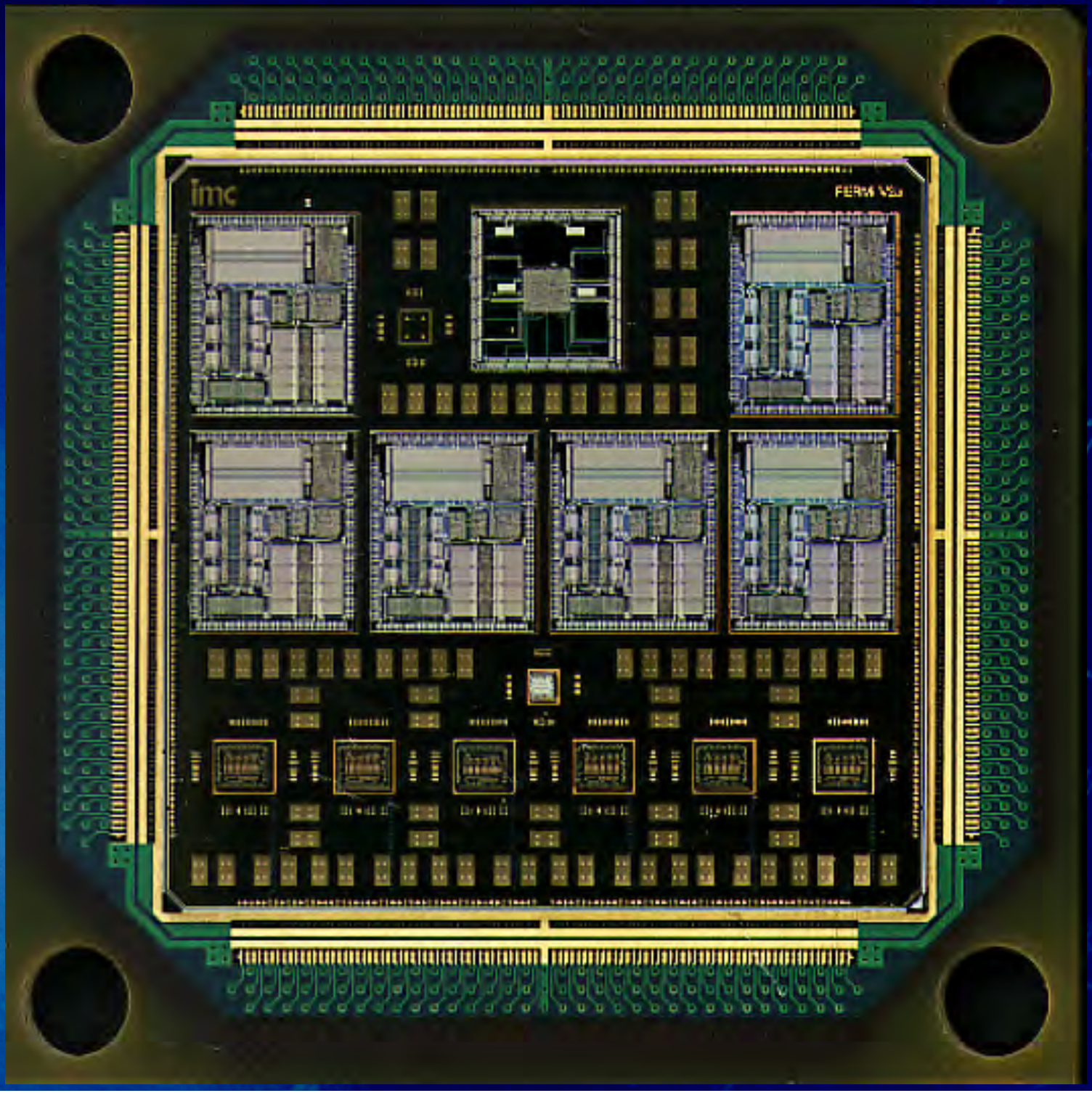
Multi Chip Modules (MCM)



multi-layer ceramic

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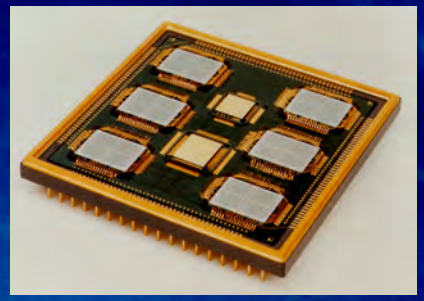
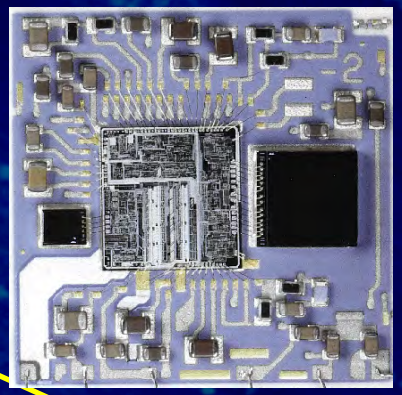
Advances in System Packaging

PCB (Printed Circuit Board)



MCM (Multi-Chip Modules)



SiP (System-in-Package)

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System-in-package (SiP)

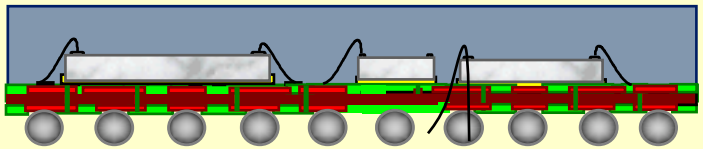
A combination of multiple active electronic components of different functionality, assembled in a single unit that provides multiple functions associated with a system or sub-system

System-in-Package (SiP)

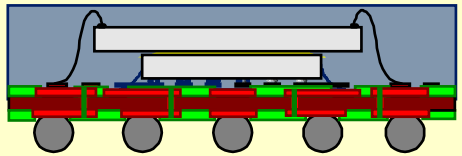
- contains more than 1 silicon die
- utilizes a substrate or carrier
- can include passive, sensors, actuators, MEMS, bio-chips, …
- works as a “functional block” or as a “sub-system”
- comes in various packaging technologies

SiP Packaging Technologies

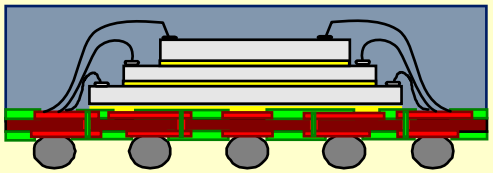
Side-by-side



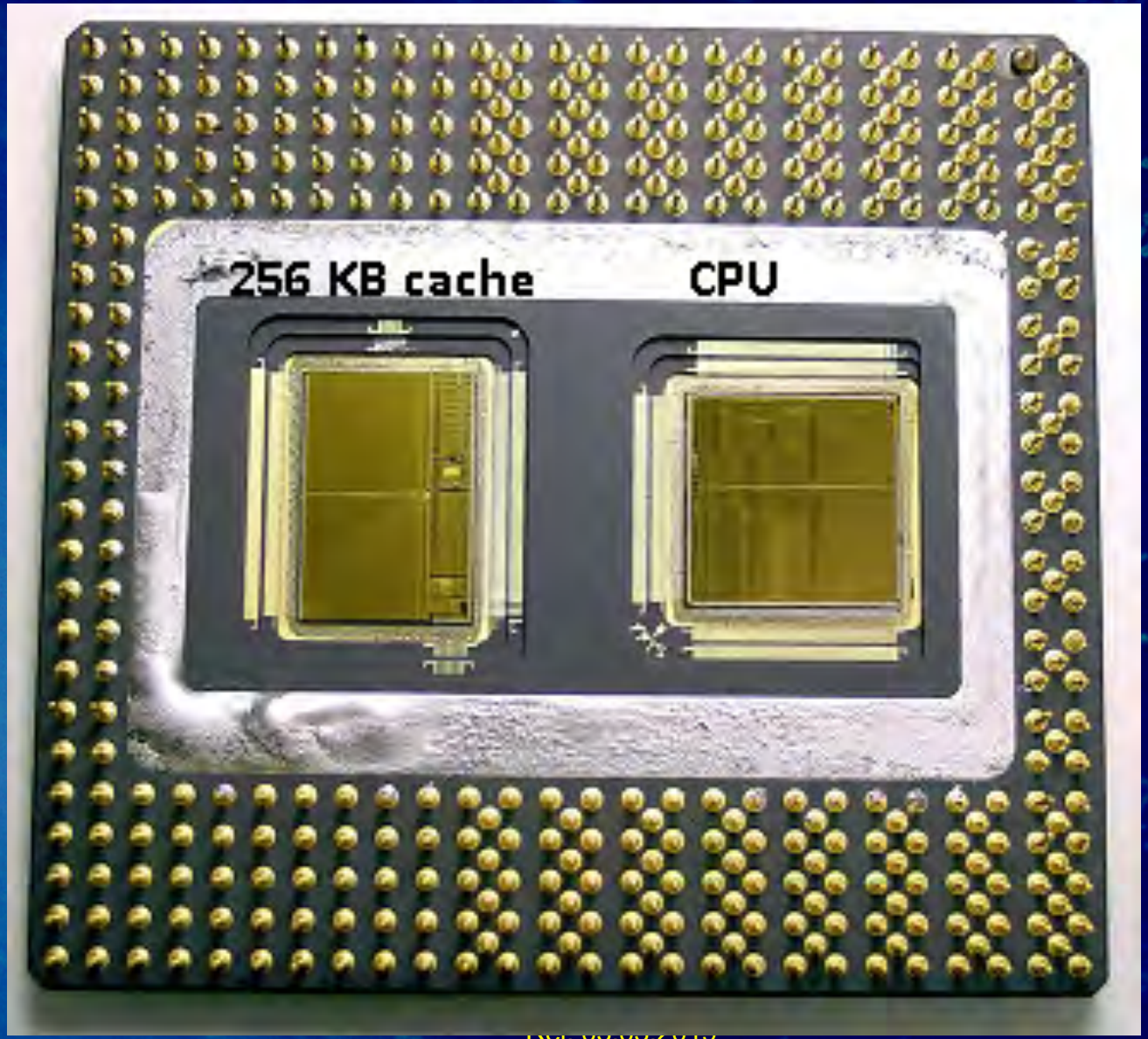
Flip Chip / Wire bond



Stacked / Wire bond



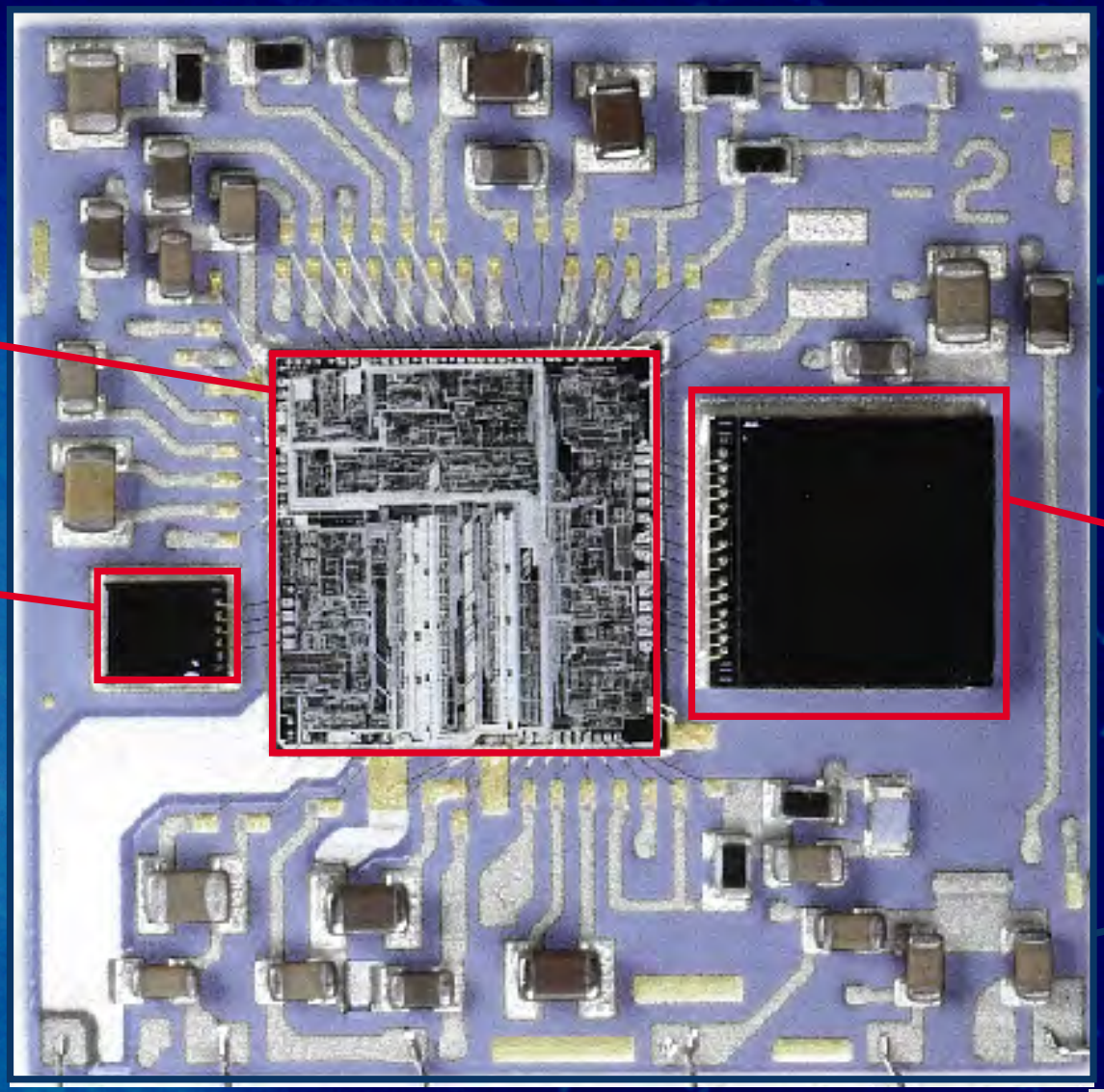
SiP : An example



SiP : An example

ASIC (Signal Processing, Bus Control)

Micromechanical Acceleration Sensor



Micromech. Yaw Rate Sensor

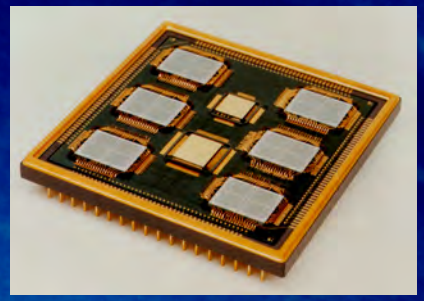
Micro hybrid Carrier

ESP-Module

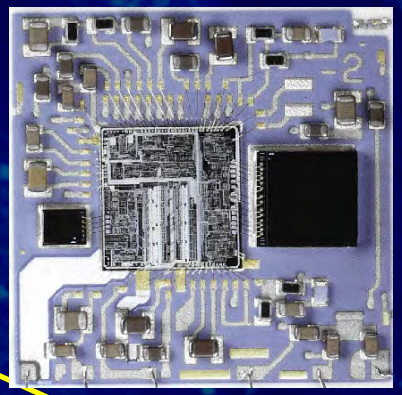
Rel. 03.03.2019

Advances in System Packaging

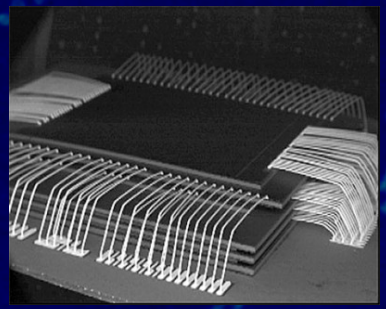
PCB (Printed Circuit Board)



MCM (Multi-Chip Modules)



SiP (System-in-Package)



3-D IC

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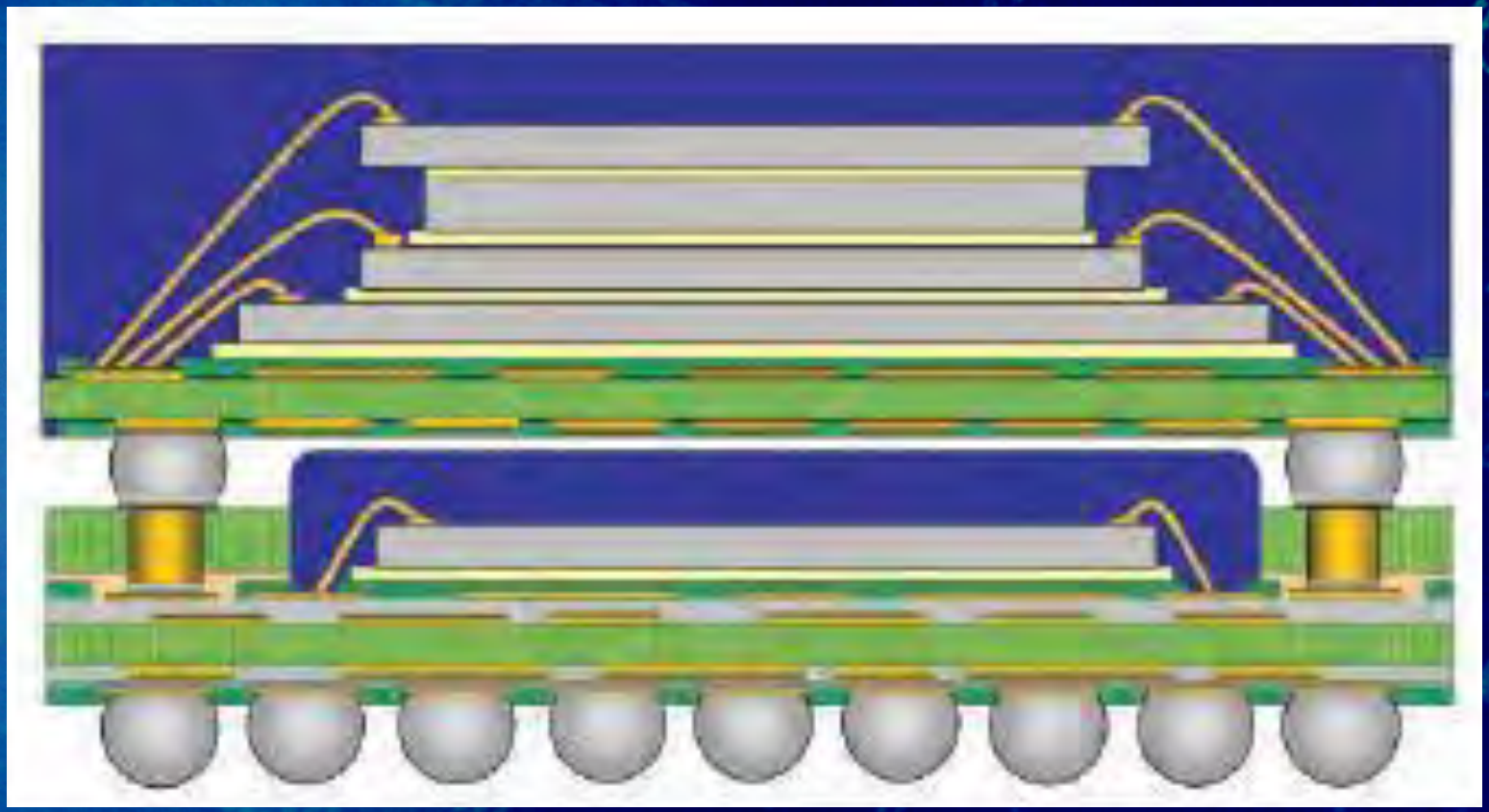
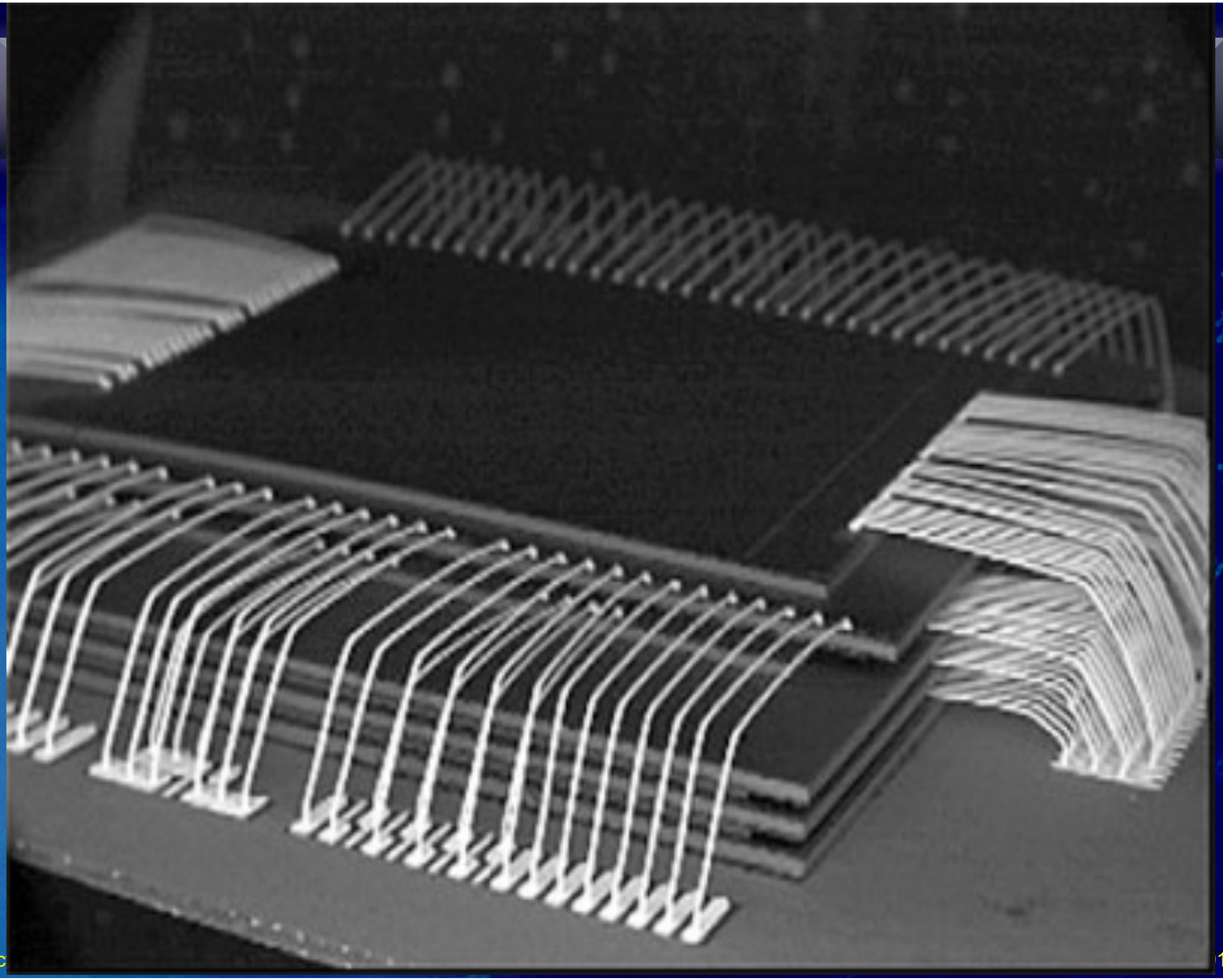
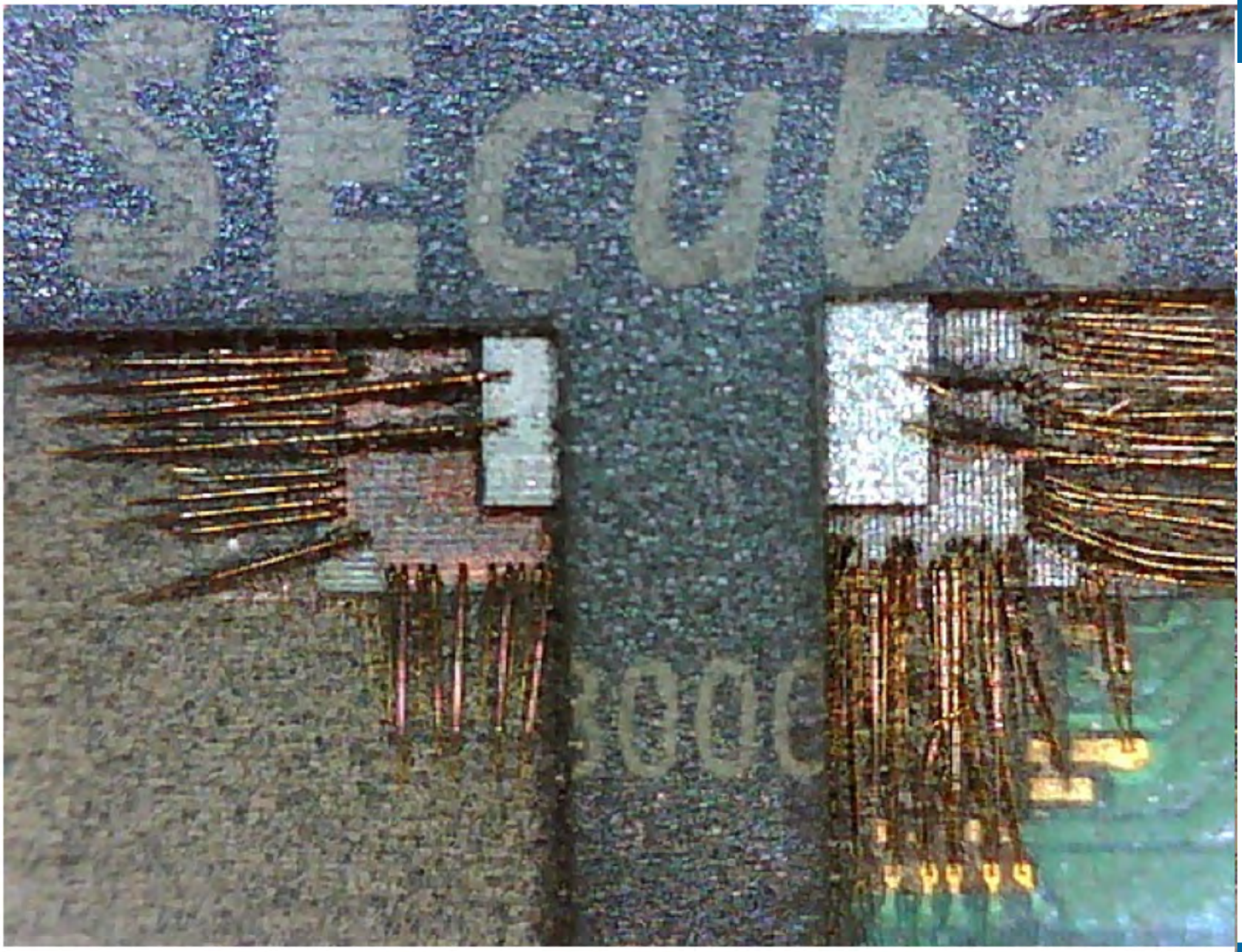
Rel. 03.03.2019

3-D IC Packaging

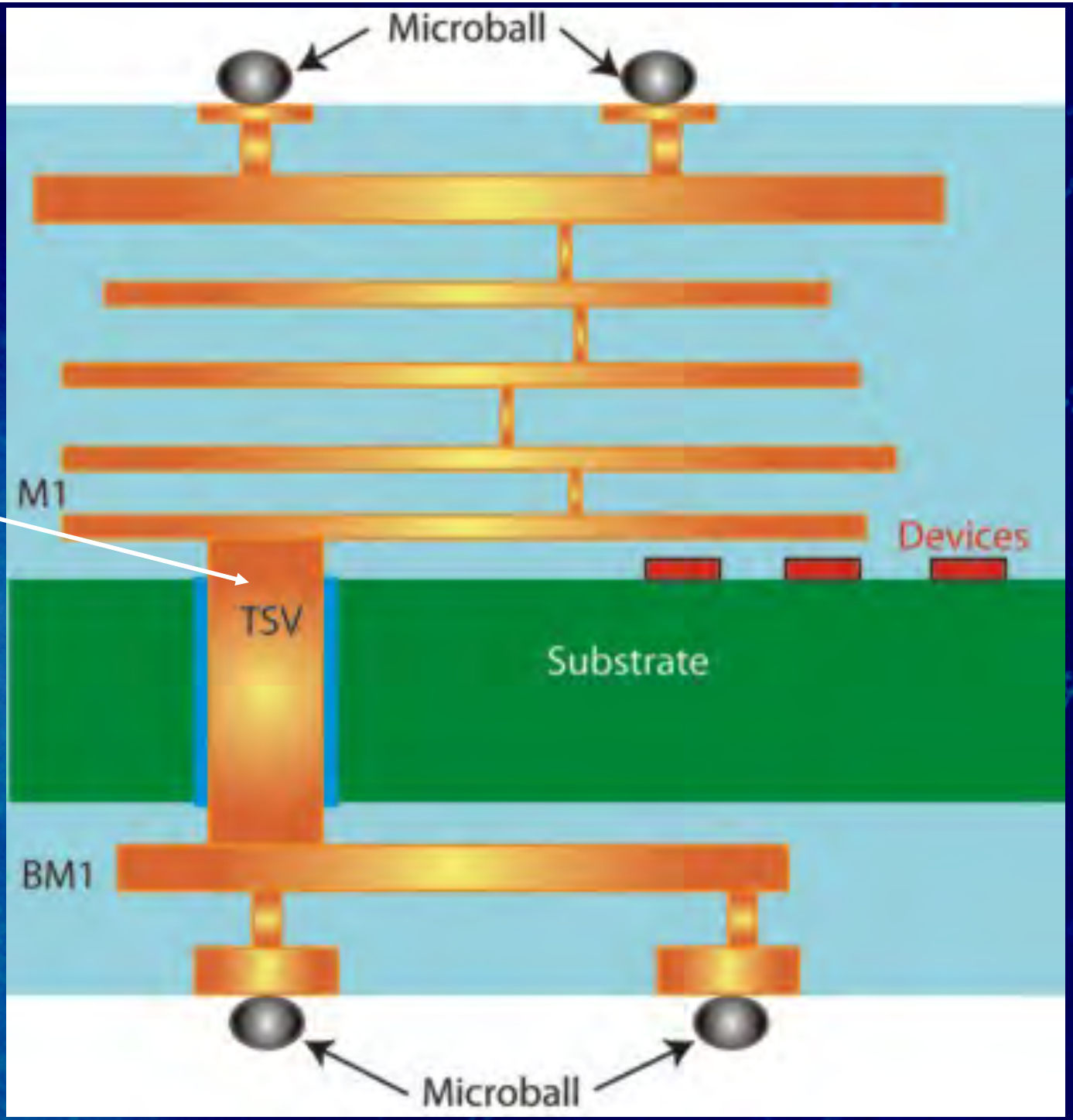
– 3-D IC Packaging is a general concept that simply means the assembly of parts in a vertical direction (typically by stacking)

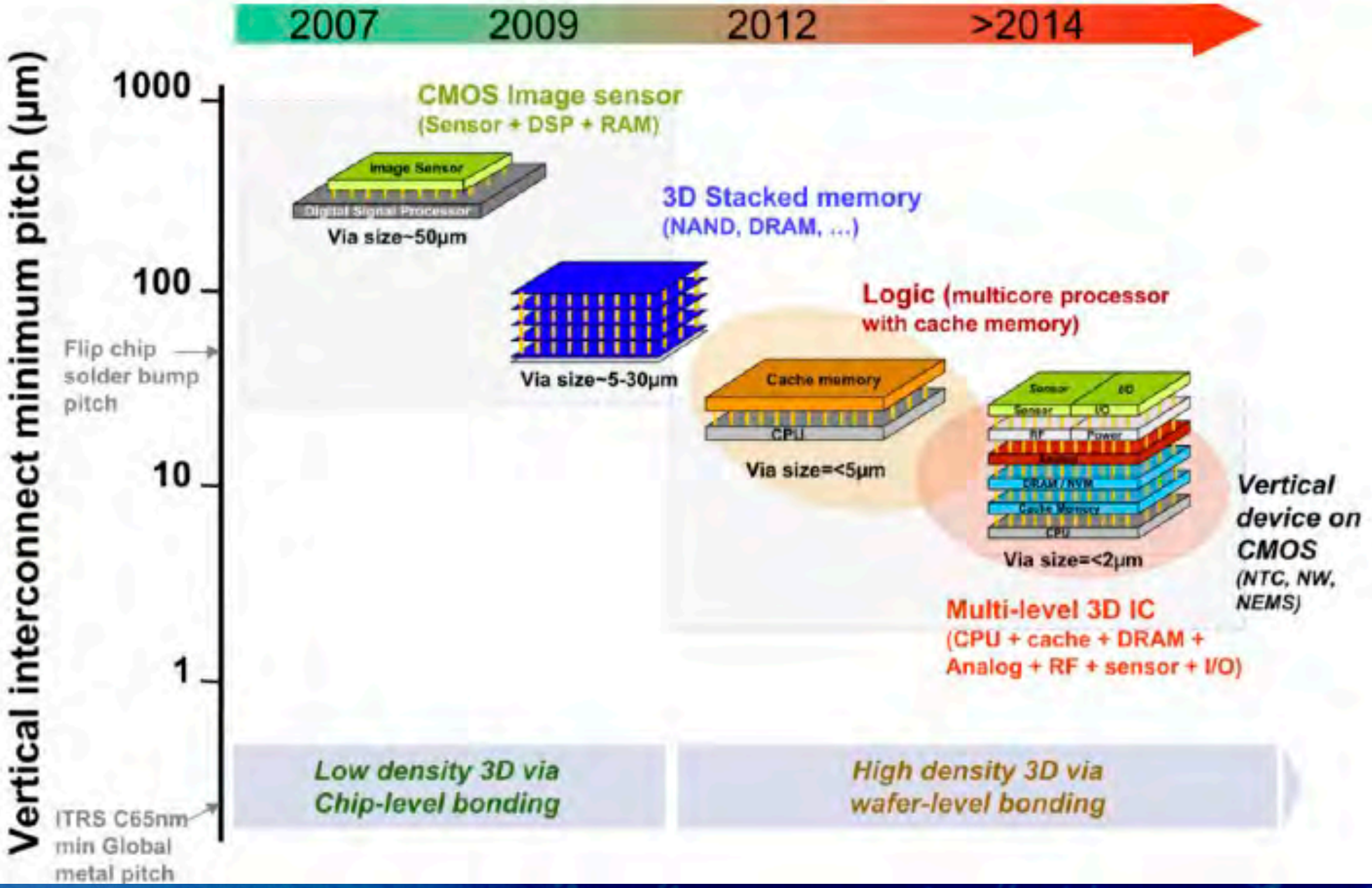




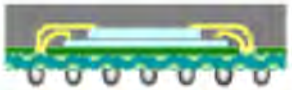
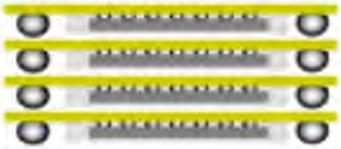


TSV (Through Silicon Via)

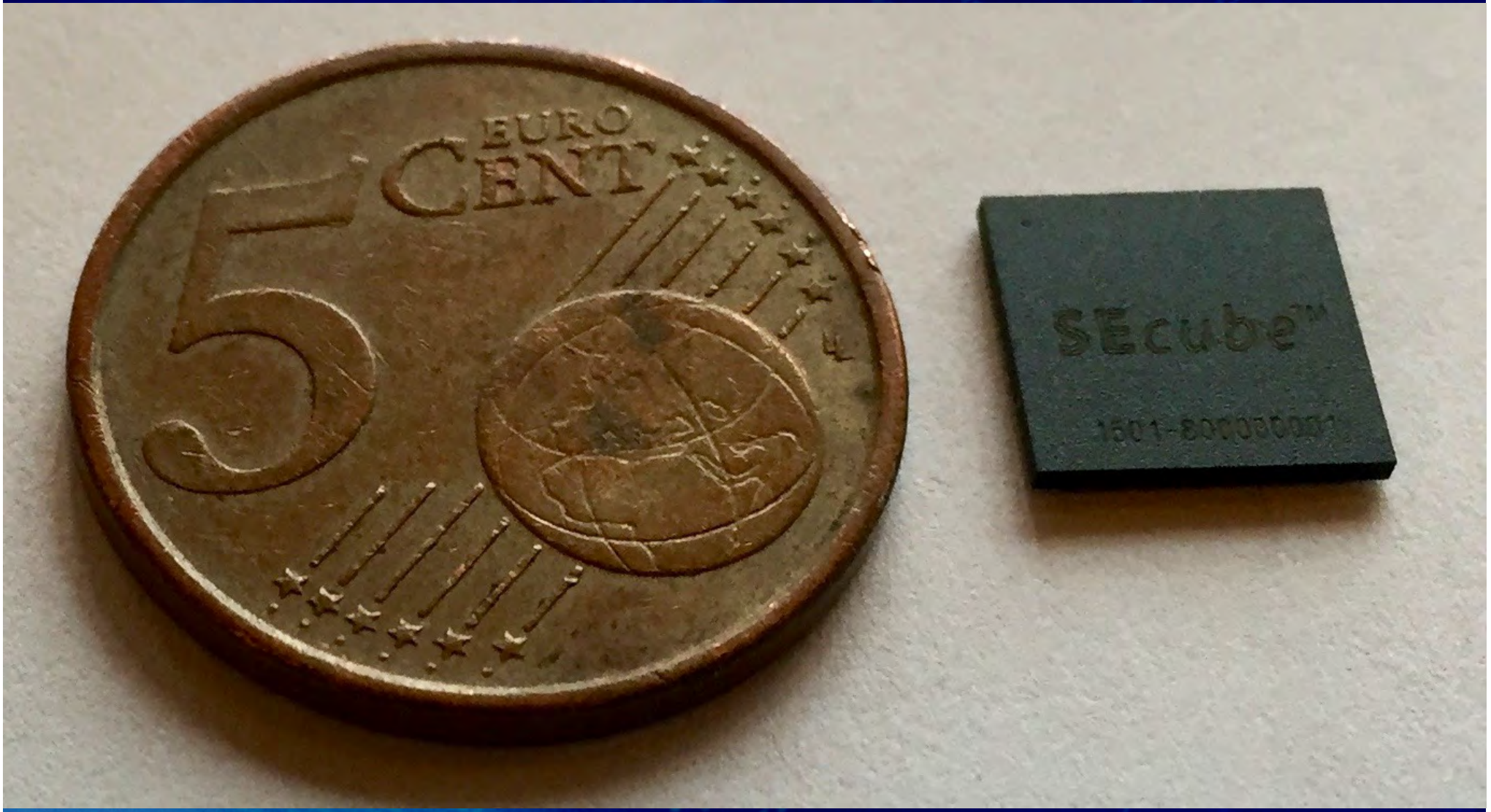




SiP Categories

Horizontal	 QFP Package	 BGA Package	 Flip Chip Module	
Stacked – **Inter-connection via substrate**	 QFP Type	 Wire Bonding Die Stacked	 Wire Bonding +Flip Chip	
	 Stacked SOP	 Package on Package	 Package in Package	
Direct connection between dice	 QFP Type	 Wire Bonding + Flip Chip (CoC)	 Through Silicon Via	
Embedded	 Chip Embedded + Package on Surface	 3D Chip Embedded type		

SEcube: a real SiP example



SEcube: a real SiP example

SE*cube*™ - *Single Chip Open Security Platform*

The first Open Security Platform in a Single Chip:

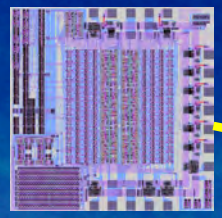
- ✓ **ARM Cortex M4, Floating Point, Low Power CPU**
- ✓ **FPGA** for Hardware Custom Developments
- ✓ **Security Controller (Smart Card)** certified EAL 6+ (SW EAL 5+)

CPU FPGA Smart Card **SE*cube*™**

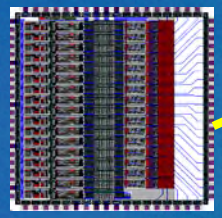
Outline

- Moore's law
- Advances in *components*:
  - System-on-Chip (SoC)
  - IP-cores
- Advances in *architectures*:
  - MPSoC
- Advances in *packaging*:
  - Advances in Device packaging
  - Advances in System packaging
- **Advances in *on-chip communications:***
  - Network-on-Chip (NoC)

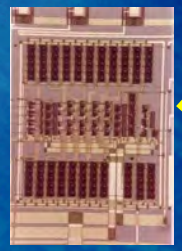
From SoC to NoC



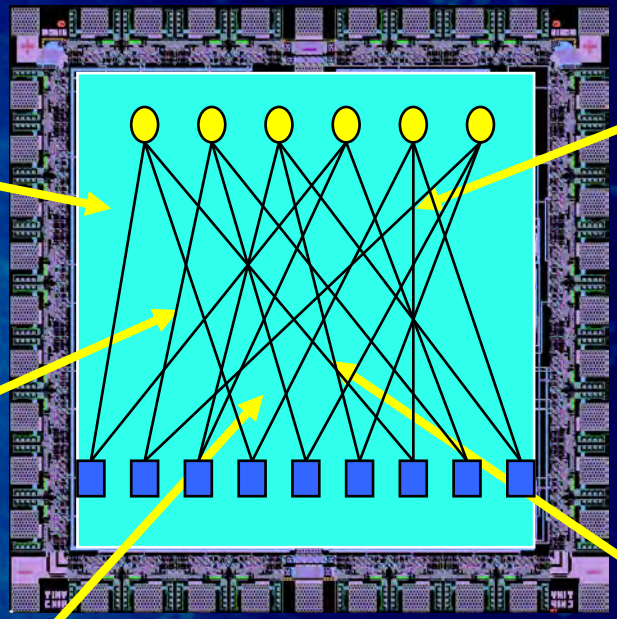
VGA CORE

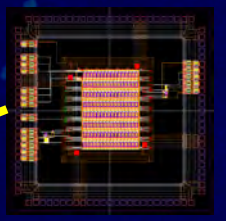


ADC / DAC



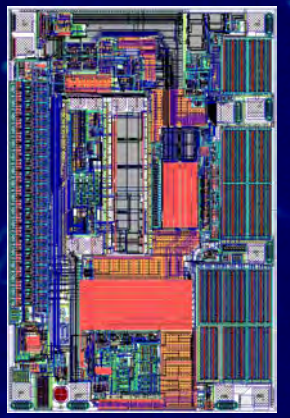
ANALOG



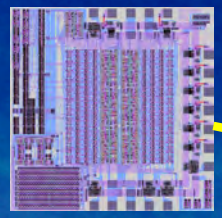


ALU CORE

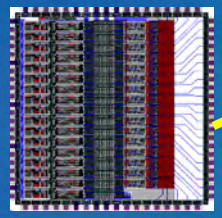
DSP



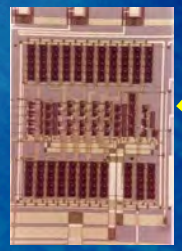
From SoC to NoC



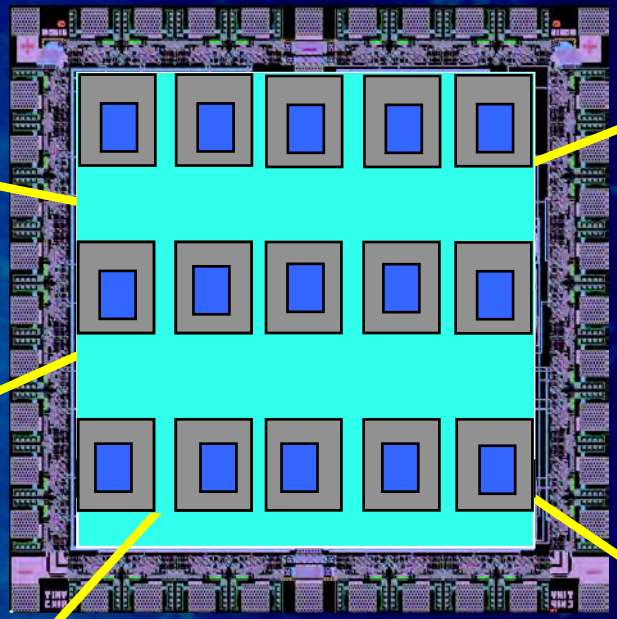
VGA CORE

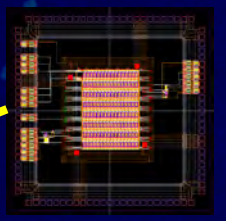


ADC / DAC



ANALOG





ALU CORE

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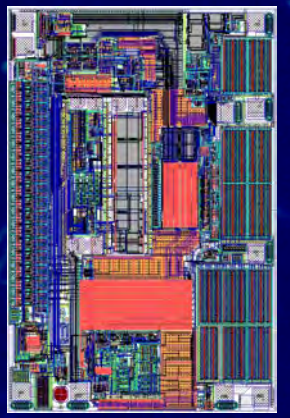
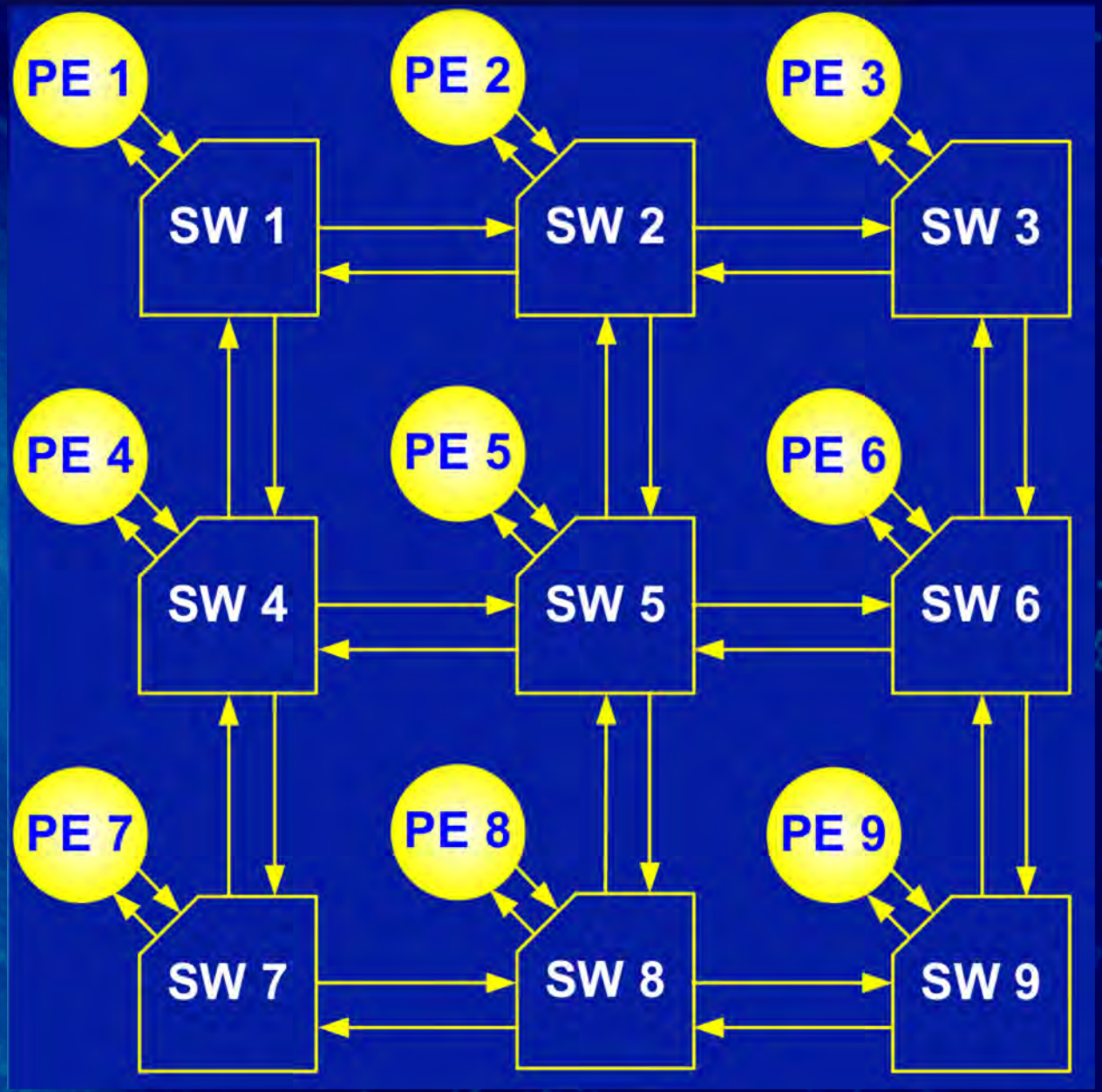


An example of 3 x 3 mesh NoC

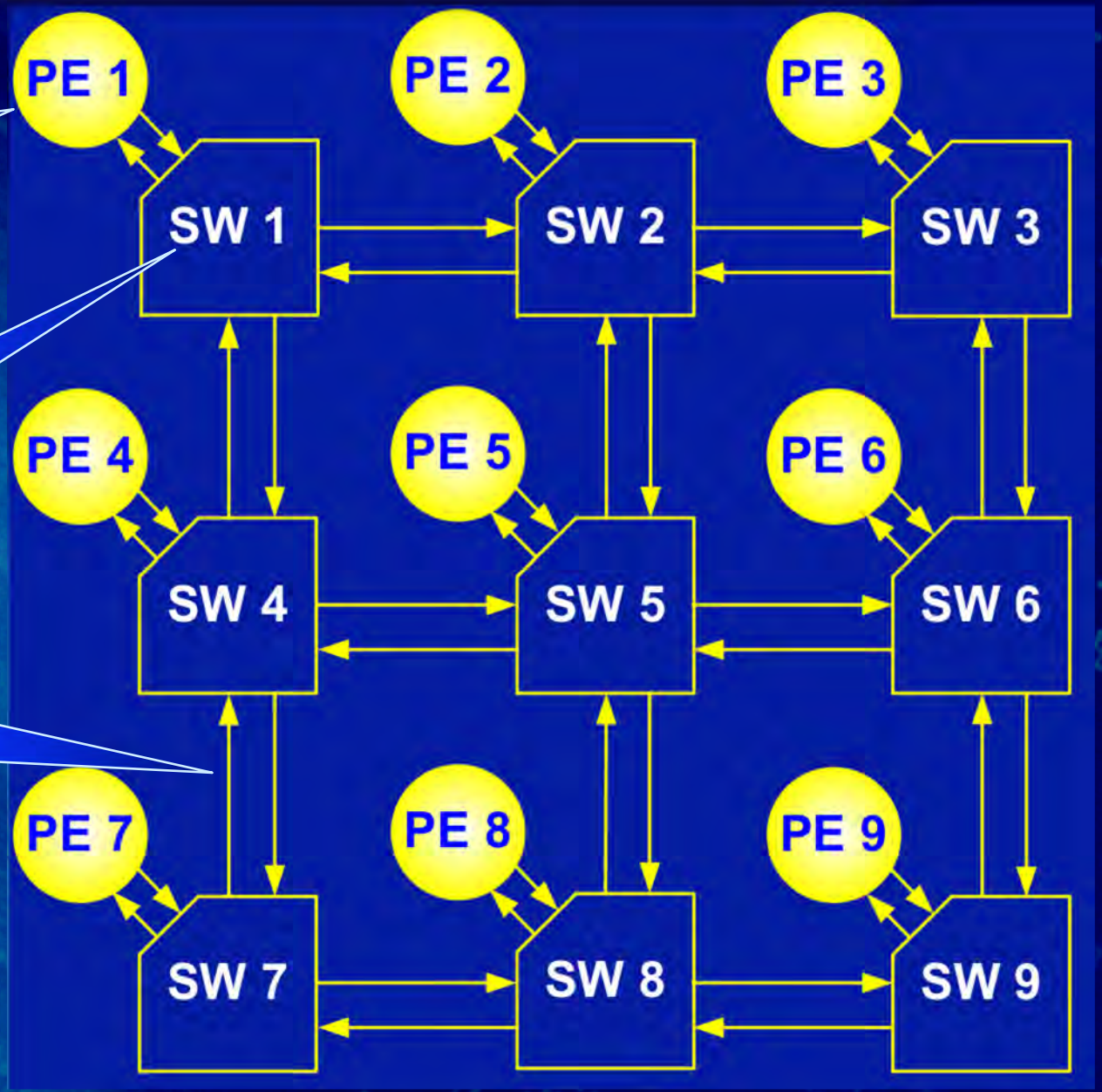


An example of 3 x 3 mesh NoC

Processing Element

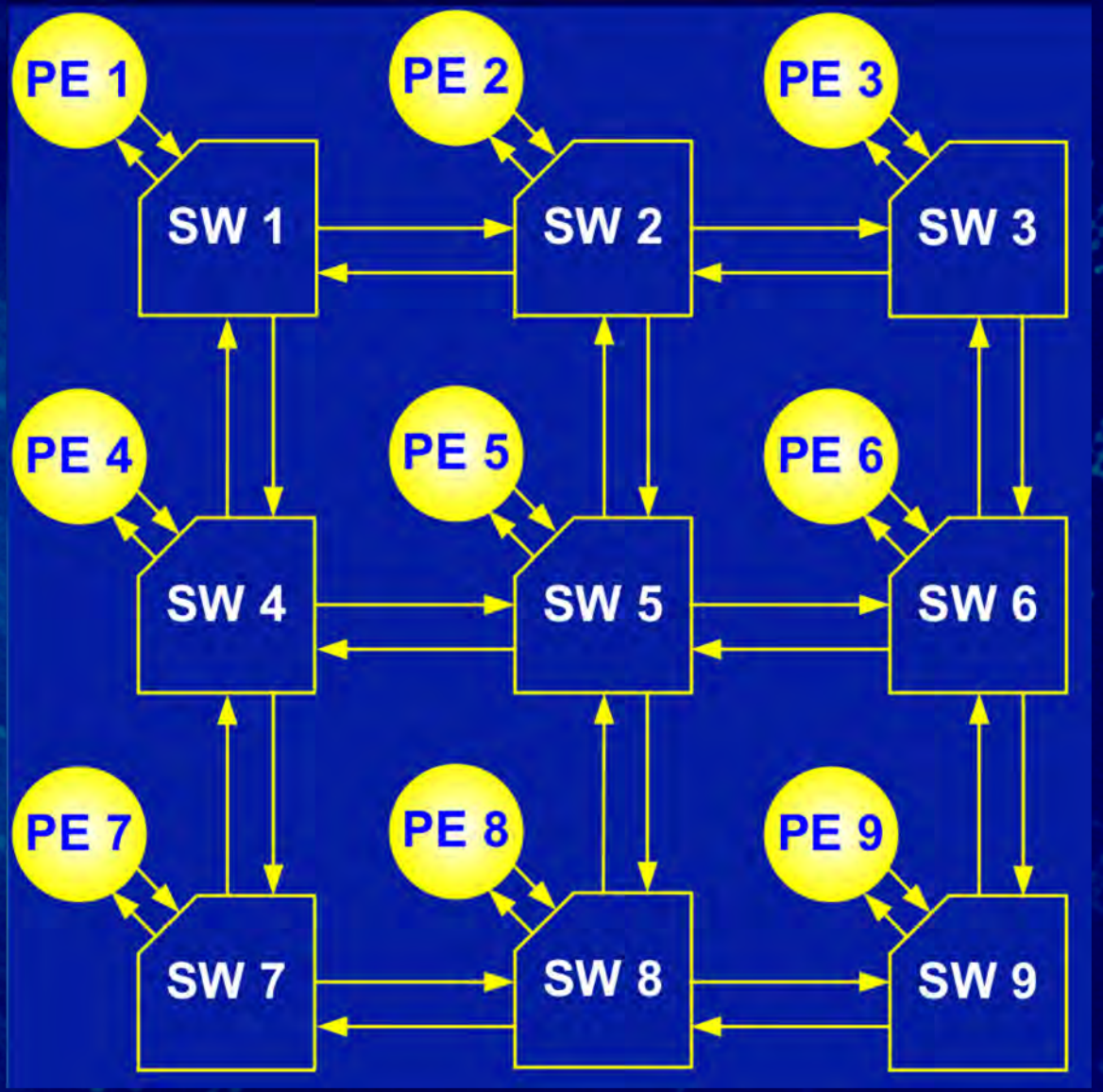
Network Switch

Packet-based network

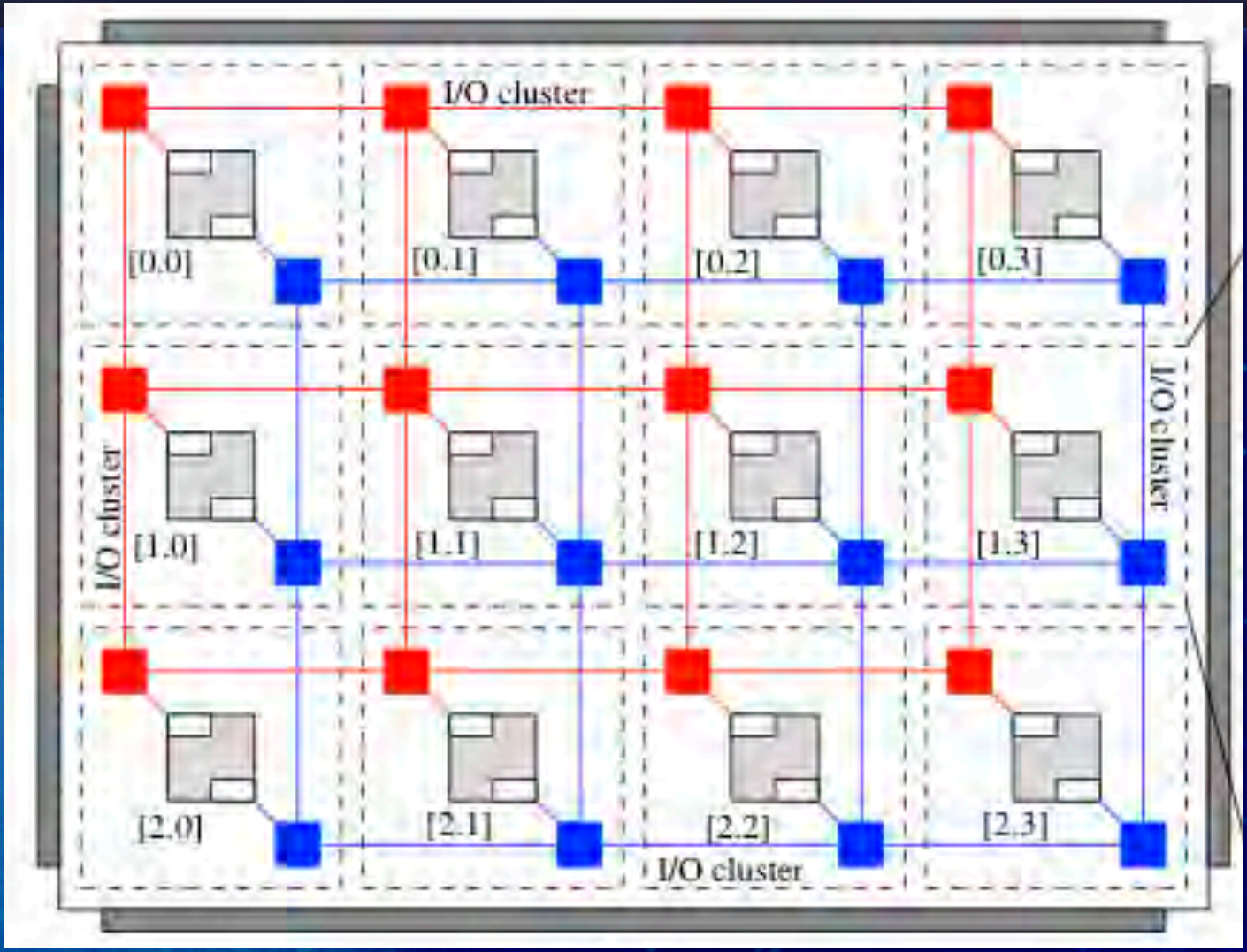


Network-On-Chip (NoC)

- Processing Elements (PEs) interconnected via packet-based network
- Processing Elements can be any type of computation unit
- Messages packetized and routed to destinations where they are de-packetized into data



An NoC based Massively Parallel Multi-Processor System-on-Chips (MP2SoCs) architecture



[University Pierre et Marie Curie, LIP6-SoC Laboratory, Paris, France]

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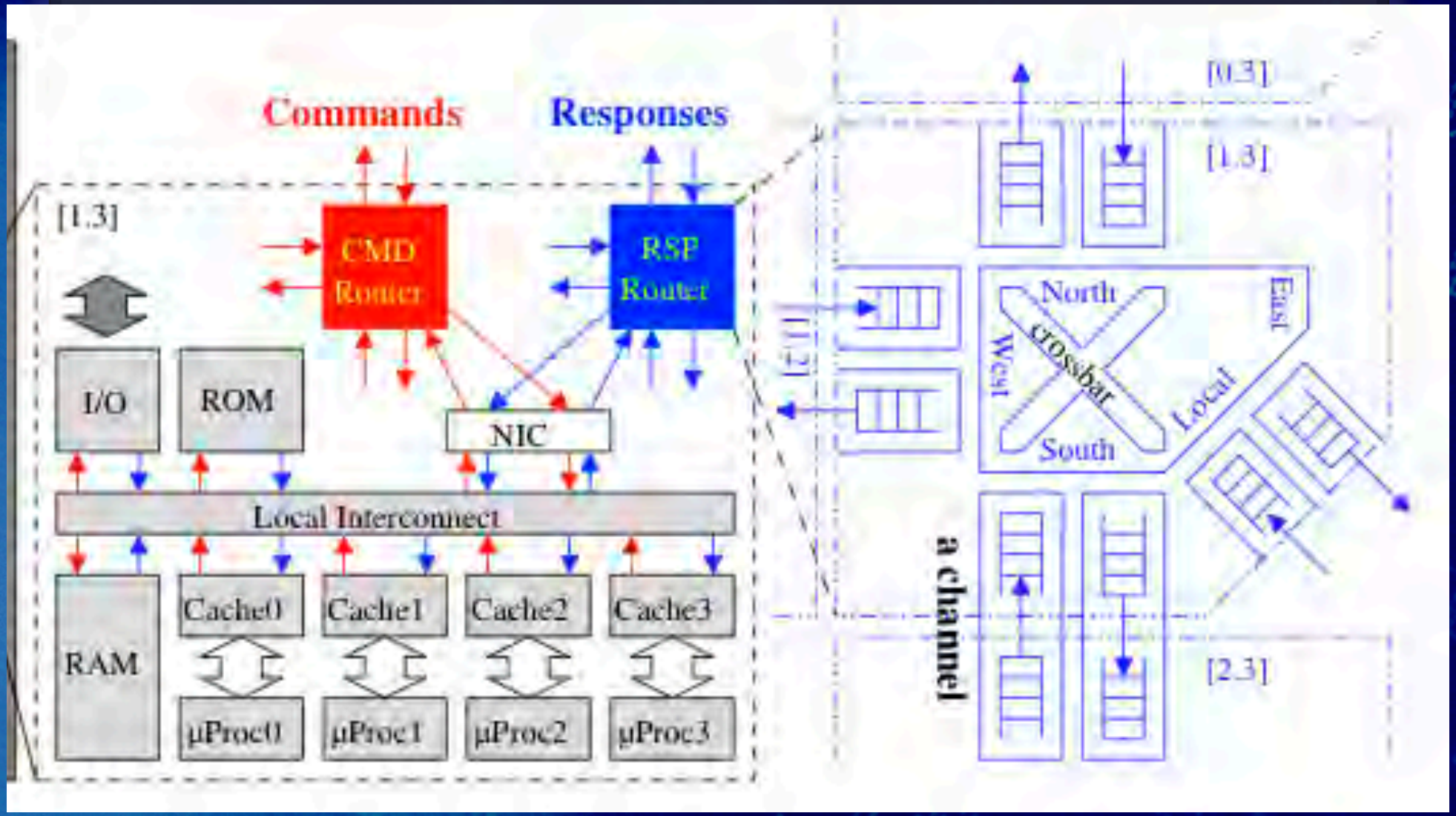
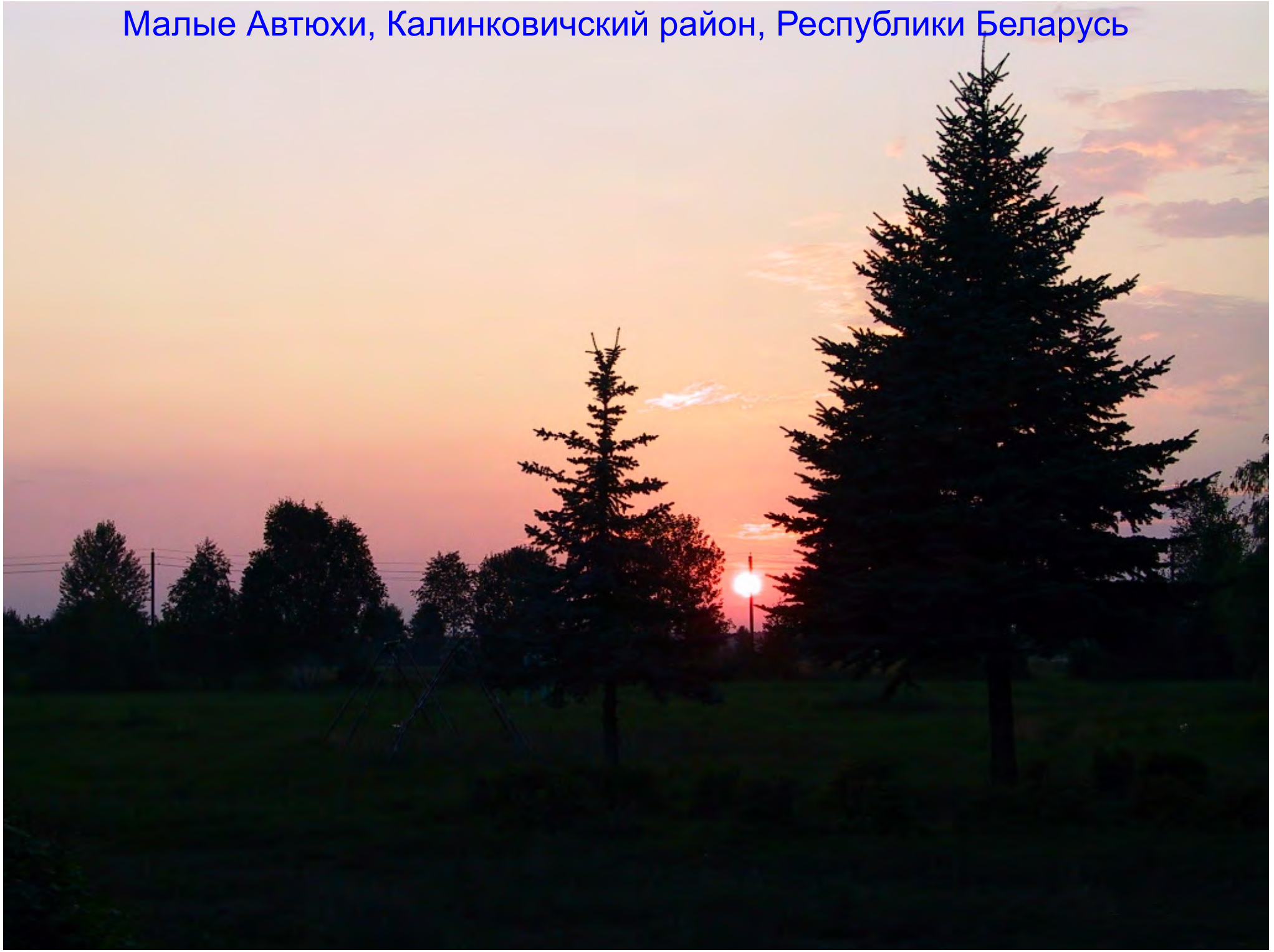


[University Pierre et Marie Curie, LIP6-SoC Laboratory, Paris, France]


Малые Автюхи, Калинковичский район, Республики Беларусь